Parallel and Distributed Processing '91

Proceedings of the Third Workshop on Parallel and Distributed Processing, WP & DP '91, Sofia, Bulgaria, 16-19 April '91

edited by Kiril Boyanov, NORTH HOLLAND, Amsterdam,1992,360 p.

ISBN 0-444-89157-9

Luminita Todor was born in Romania in 1963. She graduated in Technological Physics from the University of Bucharest in 1986, her major being in "Measurements, Testing and Control". Since 1989 she has worked with "Information Systems for Quality Assurance" Laboratory of the Research Institute for Informatics in Bucharest. She is preparing a Ph.D thesis on the subject of "Numerical Techniques and Parallelism in Simulation in Physics".

Dr. Kiril Boyanov took the mission, of at once exacting and lucid pondering, to edit the **Proceedings of the third Workshop on Parallel and Distributed Processing ,WP & DP '91**, and he accomplished it successfully. The twenty-three papers included,even though their subjects make a cluster,are largely divergent in what their approach is concerned: experiments and theory concepts, and solutions for parallel architectures,neural networks,distributed systems,transputer applications, modelling and research on computer architectures.

The table of contents included five headings under which the state-of-the-art in the field of Parallel Processing was reflected: **Parallel and Distributed Architectures, Parallel Programming, Message Routing in Parallel Architectures,Parallel Algorithms and Performance Evaluation.**

In order to let those interested share the authors' train of thoughts, short comments on each chapter are intended.

"EDS: A Host for ESQL and ElipSys" opens the volume by an overview of the architectures of EDS platform, of the advanced database system and ElipSys- the EDS logic programming system. EDS-European Declarative System- is a high performant advanced information server which extensively exploits parallelism in both hardware and software.

"Distributed Shared Memory as a Global Communication Space in a Parallel Architecture" presents an interprocess mechanism running on a parallel multicomputer architecture. Being foussed on a global identification of communicating processes and on the minimization of the interprocess communication latency, such a mechanism provides for implementing asynchronous single-buffered, synchronous non-buffered, alternative, and group communication.

The authors of **"Reconfiguration versus Static Network in Matrix Multiplication and Matrix Transpose Algorithms"** make a comparative analysis of implementations of some basic linear algebra algorithms on a reconfigurable machine. Their point is the efficiency of using dynamical reconfiguration during the program execution.

"Enhancing the Transputer Communication Model through Shared Memory", as the title shows, proposes a solution for a transputer network, by adding to the manufacturer provided transputer links, shared memory for clusters of transputers within the network. This smple hardware and software support presentation associates advantages and performances.

The paper titled " **Efficiency of Parallel and Convey Computer Systems on Execution of Algorithms for DSP**", tries to answer such a question as which is the architecture with higher performance in executing different types of algorithms for digital signal processing and image processing. The performance parameters of parallel and pipeline architectures, their results proving could make an answer.

The "**Parallel Programming**"- headed section of the volume first includes the paper " **Statistics on Storage Management in a Lazy Functional Language Implementation**", based on FAST project, of which aim is to implement a lazy functional language on a transputer array. Statistics are presnted to illustrate the lifetime characteristics of cells, a breakdown of the cells by type, and other information which is of interest to the designer of storage management system. The possibility of using ccontextual information when predicting the lifetime of an application and of vector application cells has been suggested, as well as the way this contextual information will be used.

A new notation in specifying the systems involving dynamic concurrent agents and complex linked data structures is that of Paragon, based on term graph rewriting controlled by message passing. A paper specifically deals with the "**Implementation of Paragon Specifications**", referring the Paragon language, various classifications and restrictions, which determined the translation strategy for a given Paragon specification, how specifications of the simplest static class are translated and finally, how the restrictions may be overcome with a dynamic asynchronous example.

Two approaches to validation of communication protocols are made in " **Validation of Estelle Specification**". The former is based on simulation by Ada programs, the latter- on verification using the CSP (Communicating Sequential Processes) proof system. By means of formal description techniques, developing,testing and implementing communication protocols of distributed systems will be facilitated.

"**Accurate Vector and Matrix Arithmetic for Parallel Computers**" presents several efficient implementations of some floating-point vector and matrix operations on different network architectures, for use on parallel computers.

The third section first entry is "Methods for Minimal, Adaptive and Deadlock Free Routing in Multiprocessors: A Review".While summarizing the methods for minimal, adaptive and deadlock-free routing, the authors also get them contrasted, and see to their application to a set of usual regular topologies.

The paper "**Logical Distributed Debugging in Message Passing Environment**" describes the tools necessary for testing and evaluating parallel programs in transputer arrays.

The next article is dedicated to " **A Static Routing and Synthesis Tool Based on a Heuristic Search Algorithm.**" The algorithm is executed at compile-time and supports a wide range of hardware platforms, including reconfigurable multiprocessors.

How to develop a communication facility based on reliable multicast communication in dynamic groups of processes, is the main topic of interest of the authors of the paper "**Multicast Communication in Multitransputer Systems**".With fault-tolerance in processes or link accepted, the multicast communication between groups of processes paves the way towards multiprocess system problem-solving.Typical examples of applications having multicast as a suitable paradigm are the heuristic algorithms solving, CAD multiwork station, manufacturing control, transaction processing, etc.

"**Broadcasting a Message in a Hypercube with Possible Link Faults**" is the paper inaugurating Section III of the volume,headed "**Parallel Algorithms**". Achieving what the title indicates means upgrading time complexity of a full broadcast from 0(n) to 0(n*log(n)).

Fast Fourier Transform confronts many applications and it is a difficult numerical problem to be dealt with in parallel processing. An unified approach to mapping both one-dimensional and multidimensional FFT onto MIMD is presented in the paper " **A Block-Pipelined FFT Algorithm on a Ring of Transputer**".

"**Parallel Processing of Relational Databases in a Hypercube Database Machine**" discusses parallel algorithms in multicomputer database machine with hypercube architecture. The paper shows a remarkable apprehension of all the aspects involved.

A necessary and sufficient condition that an algorithm be mapped on a linear regular array is analysed in the paper titled "**The Mapping of Algorithms on Linear Systolic Arrays**".

The last section headed as "**Performance Evaluation**" starts with the paper "**A Teamware Workbench for Concurrent Collaborative Work**". Here the framework of an asynchronous distributed environment is described, providing the basis for a computer-assisted co- operative work in the so-called groupware. A layered architecture is proposed where each individual work environment and its team work environment get integrated. Then, a PilotCard system is proposed for accessing data resources by the associative method. Such schemes help the environment of the concurrent collaborative work-named teamware work bench- be constructed.

"**Modelling and Analysing of Concurrent Systems with Extended Timed Nets**" is a presentation of a high formalism for modelling and analysis of deterministic concurrent, systems, based on ordinary conflict-free Petri nets and called **Extended Timed Nets**. After introducing the formal **ETN** model, a functional language describing both the structure and semantics of such nets comes in. Finally, a software tool for the specifications analysis and simulation by **ETN** is proposed. During simulation statistics yielded by place- and transition-related observations enable steady-state performance estimators.

A simulator under development is presented in "**Parallel Machine Simulation for the Design of Architectures for Neural Networks**".The usefulness of such a simulator will be in testing the designs of neural computers-machines which large classes of neural networks and connectionist models are efficiently simulated on.

Neural nets simulation is also delat with in the paper "**Transputer Simulation of Neural Nets and Digital Systems**". Two types of applications are considered: implement a Boltzmann machine Neural Network simulator for **Quadratic Assignment Problem** (QAP) solving, the evaluation of some digital signal processing algorithms implementation in Fast Fourier Transform (FFT). The programs are mapped onto various hardware topologies with a different number of transputers.

The papers are authored by scientists from the United Kingdom, Belgium, Germany, Greece,France, Russia annd Bulgaria. Parallel architectures, neural networks, distributed systems and high performant CAD/CAM systems get new perspectives.

Unmistakably, they are among those who originated ways of looking at transputer applications,and ways of modelling and researching on computer architectures.

Luminita Todor