Analysis and Implementation of Positive Output Super Lift Converter Using Artificial Neural Network with Sliding Mode Controller

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Abstract: This paper proposes the control of split capacitor type elementary additional series positive output super lift converter (SEPOSLC) by using artificial neural-network (ANN) with sliding mode controller. This converter implements the output voltage increase in geometric sequence and enhances the voltage transfer gain in power law. The ANN controller is trained to control the converter so that it produces constant output voltage irrespective of change in the input voltage. ANN with sliding mode control (SMC) is proposed for this converter with a view to controlling voltage ripple. The precision of the proposed system is analyzed in comparison with various controllers such as the ANN controller, Fuzzy logic controller, and conventional PI controller. In order to validate the effectiveness of the proposed system, it is implemented in hardware with linear and nonlinear loads.

Keywords: ANN, ANN with sliding mode controller, BLDC motor, FLC, PI, SEPOSLC.

1. Introduction

Nowadays DC-DC converters play a major role in the world of power electronics. Theoretically, the basic DC–DC converters like the boost, buck–boost, Cuk, single-ended primary inductor converter (SEPIC), etc., can reach peak step-up voltage transfer gain with an enormous high duty cycle (Tran et al., 2018), (Lu, Cheng & Lee, 2003). Unfortunately, in practice, the step-up voltage gain is bounded due to the outcome of power switches, rectifier diodes and the equivalent series resistance (ESR) of inductors and capacitors. Moreover, the extremely high Duty-cycle process will tend to a major reverse retrieval problem (Nguyen et al., 2018).

Positive output super-lift converters (Luo & Ye, 2003) are a series of attractive DC–DC topologies, which provides very high step-up voltage transfer gains due to cascade connection and the transformerless operation. Super-lift converters utilize the voltage lift (VL) technique, which is an effective method broadly used in electronic circuit design (Zhu & Luo, 2009), for understanding the throughput improvement.

Super-lift (SL) technique implements the output voltage increase step by step in the geometric progression (El-Ghanam, 2020). It effectively enhances the voltage transfer gain in power series. There are two such subseries in super lift converters namely main series and additional series. The main series is categorized into the elementary circuit, relift circuit, and triple-lift circuit. Additional series are extracted from the corresponding circuits of the main series.

The PI controller design has been limited for many years (Alvarez-Ramirez et al., 2001), (Garcerá et al., 2004). The choice of the elements of control system is a tradeoff between robustiousness and quick transient outcome. The fuzzy control system is a mathematical control system capable of dealing with imprecise data and it is analyzed by various researchers for controlling DC-DC converter (Elmas et al., 2009), (Gupta et al., 1997), (Guo et al., 2011). An alternative sketch technique for recognizing and controlling these systems was presented by (Seshagiri & Khalil 2000), (Shoja-Majidabad & Hajizadeh 2020) (Hassan & Kothapalli, 2012) by the neural-network-based control method.

Though DC–DC converters are typical variable structure systems, for controlling such system variable structure control namely sliding mode (SM) control (Goudarzia & Khosravi, 2018), (Repecho et al., 2018), (Tan & Lai, 2008) is the suitable one. Hence, in this study SMC is employed along with ANN controller for potential control in SEPOSLC.

The organization of this research article is as follows: Section 2 describes working of SEPOSLC converter. Modeling of transfer function of SEPOSLC Converter is presented in Section 3. Section 4 discusses PI controller based SEPOSLC Converter. Fuzzy logic controller for SEPOSLC is presented in section 5. Section 6 sets forth ANN controller-based converter. Section 7 puts forward ANN with SMC controller based SEPOSLC

Converter. Section 8 addresses SEPOSLC with inverter fed brushless DC (BLDC) motor. Section 9 presents the results attained from the simulation analysis. Section 10 sets forth the detailed result of experimental analysis and finally Section 11 presents the conclusion of this article.

2. Working of SEPOSLC Converter

The schematic illustration of SEPOSLC converter contains both the active and passive components represented in the Figure 1(a). The active voltage supply for SEPOSLC converter is a DC power source V_{in}. Resistor R_0 is a load, capacitors C_1, C_2, C_3, C_4, C_5, and inductor L_1 are the passive parameters of SEPOSLC converter. N-channel *metal-oxide-semiconductor field-effect transistor* (MOSFET) switch and freewheeling diodes are the power switching components contained in the SEPOSLC circuit for moving the current in the DC bias.

(a)

(b)

(c)
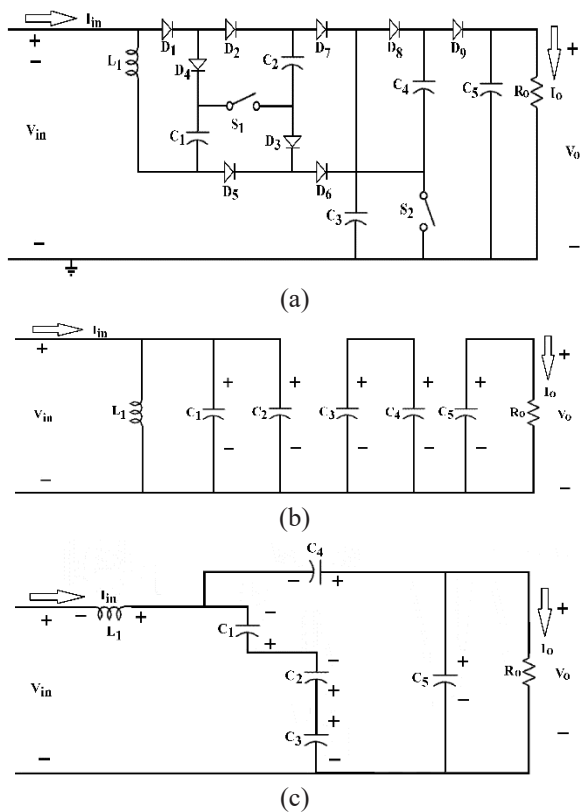
Figure 1. (a). Schematic layout of split capacitor type elementary additional series positive output super lift converter, (b) Schematic layout for mode 1 (ON state) of SEPOSLC converter, (c) Schematic diagram for mode 2 (OFF state) of SEPOSLC converter

There are two n-channel MOSFETs S_1 and S_2 implemented in the SEPOSLC converter. In the converter schematic the resistor R_0 is assumed as load resistance. $D_1, D_2, D_3, D_4, D_5, D_6, D_7, D_8, D_9$

are the nine diodes present in the schematic diagram. On the time of switching condition, forwarding of current is precisely done by using diodes in the converter schematic diagram.

It is assumed that the split capacitor type elementary additional series positive output super lift converter works in ideal state and continuous conduction mode. There are two switching modes that the converter schematic will undergo (Leyva et al., 1997). When the switch S_1 is closed and S_2 is open SEPOSLC converter achieves mode 1. When the switch S_1 is open and S_2 is closed SEPOSLC converter attains mode 2. The schematic layout of SEPOSLC converter is represented for both modes. For both mode 1 (ON state) and mode 2 (OFF state) the state space illustration of the SEPOSLC schematic is designed.

By adding up the ON system matrix with (1-*k*) the OFF system matrix, the system matrix illustration of the whole split capacitor type elementary additional series positive output super lift converter schematic is acquired. The SEPOSLC state matrix using state space to transfer function conversion formula in MATLAB software for the transfer function is acquired. The stability of the acquired transfer function is described by Bode plot and root locus. The conversion of state space to transfer function through the common coding is stated below.

$$[b,a] = sstof (A,B,C,D) \qquad (1)$$

Report on MODE 1 (ON State)

The schematic layout of SEPOSLC converter in mode 1 (ON state) is shown in the Figure 1(b). When the input voltage V_{in} is applied to the capacitors C_1 and C_2, capacitors get charged to achieve the steady state condition. When V_{in} is given in this mode, the flow of current via the inductor L_1 will rise. The switching time for mode 1 (ON state) is kT (Venkatesh & Kamalakannan, 2016).

Using the electrical circuit analysis, the state space illustration for mode 1 of split capacitor type elementary additional series positive output super lift converter is acquired. A 6×6 matrix is developed for the system matrix for the mode 1, because the schematic diagram includes six passive components. The state matrix (A), input matrix (B), output matrix (C) and feedthrough matrix (D) make up the system matrix. The state space representation in the Standard formula is stated below.

$$\frac{dx(t)}{dt} = Ax(t) + Bu(t) \tag{2}$$

$$y(t) = Cx(t) + Du(t) \tag{3}$$

Equations (4) and (5) express the system matrix for mode 1 SEPOSLC schematic

$$\frac{d}{dt}\begin{pmatrix} i_{L1} \\ V_{c1} \\ V_{c2} \\ V_{c3} \\ V_{c4} \\ V_{c5} \end{pmatrix} =$$

$$= \begin{pmatrix} 0 & -\dfrac{1}{L_1} & 0 & 0 & 0 & 0 \\ -\dfrac{1}{C_1} & 0 & -\dfrac{C_2}{C_1} & 0 & 0 & 0 \\ -\dfrac{1}{C_2} & -\dfrac{C_1}{C_2} & 0 & -\dfrac{C_3}{C_2} & 0 & 0 \\ \dfrac{1}{C_3} & \dfrac{C_1}{C_3} & \dfrac{C_2}{C_3} & 0 & -\dfrac{C_4}{C_3} & 0 \\ \dfrac{1}{C_4} & \dfrac{C_1}{C_4} & \dfrac{C_2}{C_4} & \dfrac{C_3}{C_4} & 0 & \dfrac{C_5}{C_4} \\ \dfrac{1}{C_5} & \dfrac{C_1}{C_5} & \dfrac{C_2}{C_5} & \dfrac{C_3}{C_5} & \dfrac{C_4}{C_5} & 0 \end{pmatrix} \begin{pmatrix} i_{L3} \\ V_1 \\ V_2 \\ V_3 \\ V_4 \\ V_5 \end{pmatrix} + \tag{4}$$

$$+ \begin{pmatrix} \dfrac{1}{L_1} \\ \dfrac{1}{R_{in}C_1} \\ \dfrac{1}{R_{in}C_2} \\ 0 \\ 0 \\ 0 \end{pmatrix} V_{in}$$

$$V_0 = \begin{pmatrix} 0 & 0 & 0 & 0 & 0 & \dfrac{1}{R_0 C_5} \end{pmatrix} \begin{pmatrix} i_{L1} \\ V_1 \\ V_2 \\ V_3 \\ V_4 \\ V_5 \end{pmatrix} + V_{in} \tag{5}$$

Report on MODE 2 (OFF State)

The schematic diagram for SEPOSLC converter under mode 2 condition is shown in Figure 1(c). When the input voltage V_{in} is applied to the capacitors C_1 and $C_{4,}$ capacitors get charged to achieve the steady state condition. When V_{in} is given in this mode, the flow of current via the inductor L_1 decreases. The switching time of mode 2 (OFF state) is $(1 - kT)$.

Using the electrical circuit analysis, the state space illustration for the mode 2 of split capacitor type elementary additional series positive output super lift converter is acquired. A 6×6 matrix is formed for the system matrix for mode 2, because of the six passive components inside the circuit. The state matrix (A), input matrix (B), output matrix (C) and feedthrough matrix (D) make up the system matrix. The system matrix is represented in the General formula which is stated below.

In equations (6) and (7) the state space representation for the mode 2 SEPOSLC circuit is shown.

$$\frac{d}{dt}\begin{pmatrix} i_{L1} \\ V_{c1} \\ V_{c2} \\ V_{c3} \\ V_{c4} \\ V_{c5} \end{pmatrix} =$$

$$= \begin{pmatrix} 0 & \dfrac{-1}{L_1} & 0 & 0 & 0 & 0 \\ \dfrac{1}{C_1} & 0 & 0 & 0 & -\dfrac{C_4}{C_1} & 0 \\ \dfrac{1}{C_2} & \dfrac{C_1}{C_2} & 0 & -\dfrac{C_3}{C_2} & 0 & 0 \\ \dfrac{1}{C_3} & \dfrac{C_1}{C_3} & \dfrac{C_2}{C_3} & 0 & -\dfrac{C_4}{C_3} & 0 \\ \dfrac{1}{C_4} & \dfrac{C_1}{C_4} & \dfrac{C_2}{C_4} & \dfrac{C_3}{C_4} & 0 & -\dfrac{C_5}{C_4} \\ \dfrac{1}{C_5} & \dfrac{C_1}{C_5} & \dfrac{C_2}{C_5} & \dfrac{C_3}{C_5} & \dfrac{C_4}{C_5} & 0 \end{pmatrix} \begin{pmatrix} i_{L3} \\ V_1 \\ V_2 \\ V_3 \\ V_4 \\ V_5 \end{pmatrix} + \tag{6}$$

$$+ \begin{pmatrix} \dfrac{1}{L_1} \\ \dfrac{1}{R_{in}C_1} \\ \dfrac{1}{R_{in}C_2} \\ \dfrac{1}{R_{in}C_3} \\ \dfrac{1}{R_{in}C_4} \\ 0 \end{pmatrix} V_{in}$$

$$V_0 = \begin{pmatrix} 0 & 0 & 0 & 0 & 0 & \dfrac{1}{R_0 C_5} \end{pmatrix} \begin{pmatrix} iL_1 \\ V_1 \\ V_2 \\ V_3 \\ V_4 \\ V_5 \end{pmatrix} + V_{in} \tag{7}$$

3. Modeling of Transfer Function of SEPOSLC Converter

Equations (8), (9), (10) show the entire state space representation of the split capacitor type elementary additional series positive output super lift converter

$$T(S) = \text{ON state matrix} + (1-k) \text{ OFF state matrix} \qquad (8)$$

Expression (9) is attained by substituting ON state and times OFF state matrix in equation (8). The complete SEPOSLC schematic state matrix and the output matrix is the sum of ON state matrix with (1-k) times OFF state matrix. The resistor value is 50Ω, each capacitor value $(C_1, C_2, C_3, C_4, C_5)$ is 30μF and inductor L_1 of 100μH are considered for acquiring the transfer function of the split capacitor type elementary additional series positive output super lift converter.

C_1-C_5. The acquired transfer function is expressed as follows (12).

$$L = \frac{V_{in}.k.T}{\Delta I_L} \qquad (12)$$

The obtained transfer function is given below equation (13).

Let M = Top Row, N = Bottom Row, then $T(s)$ = M/N

$M = 3.704*10^{11}s^2 + 1.235*10^{22}s + 2.877*10^{11}$,

$N = s^6 + 1.693*10^9 s^5 + 5.789*10^{10} s^4 + 2.483*$
$\quad *10^{15}s^3 + 8.029*10^{19}s^2 + 1.235*10^{22}s$, then

$$T(s) = M / N \qquad (13)$$

It can be noticed that, on the time of switch OFF state the inductor current decreases and on the time

$$\frac{d}{dt}\begin{pmatrix} i_{L1} \\ V_{c1} \\ V_{c2} \\ V_{c3} \\ V_{c4} \\ V_{c5} \end{pmatrix} = \begin{pmatrix} 0 & \frac{k-2}{L_1} & 0 & 0 & 0 & 0 \\ \frac{-k}{C_1} & 0 & \frac{-C_2}{C_1} & 0 & -\frac{C_4(1-k)}{C_1} & 0 \\ \frac{-k}{C_2} & \frac{-kC_1}{C_2} & 0 & \frac{C_3(k-2)}{C_2} & 0 & 0 \\ \frac{2-k}{C_3} & \frac{C_1(2-k)}{C_3} & \frac{C_2(2-k)}{C_3} & 0 & \frac{-kC_4}{C_3} & 0 \\ \frac{2-k}{C_4} & \frac{C_1(2-k)}{C_4} & \frac{C_2(2-k)}{C_4} & \frac{C_3(2-k)}{C_4} & 0 & \frac{kC_4}{C_5} \\ \frac{2-k}{C_5} & \frac{C_1(2-k)}{C_5} & \frac{C_2(2-k)}{C_5} & \frac{C_3(2-k)}{C_5} & \frac{C_4(2-k)}{C_5} & 0 \end{pmatrix} \begin{pmatrix} i_{L1} \\ V_1 \\ V_2 \\ V_3 \\ V_4 \\ V_5 \end{pmatrix} + \begin{pmatrix} \frac{2-k}{L_1} \\ \frac{2-k}{R_{in}C_1} \\ \frac{2-k}{R_{in}C_2} \\ \frac{1-k}{R_{in}C_1} \\ \frac{1-k}{R_{in}C_4} \\ \frac{1-k}{R_{in}C_4} \end{pmatrix} V_{in} \qquad (9)$$

$$V_0 = \begin{pmatrix} 0 & 0 & 0 & 0 & 0 & \frac{1}{R_0 C_5} \end{pmatrix} \begin{pmatrix} iL_1 \\ V_1 \\ V_2 \\ V_3 \\ V_4 \\ V_5 \end{pmatrix} + V_{in} \qquad (10)$$

The values of inductor L_1 and capacitor $C_1 - C_5$ are given below

$$C_i = \frac{(1-k)V_O}{f * \Delta V_O * R_0} \qquad i = 1, 2 .., 5 \qquad (11)$$

where f is switching frequency, ΔV_O is the voltage ripple. Equation (11) is employed for all capacitors

of switch ON state inductor current increases; the upcoming equations show the peak-to-peak inductor ripple current (Δ_{iL}) and voltage transfer gain.

$$\Delta_{iL} = \frac{V_{in}}{L}kT = \frac{V_o - V_1 - V_{in}}{L}(1-k)T \qquad (14)$$

$$V_0 = \left(\frac{1}{1-k} + \frac{3-2k}{1-k} \right) V_{in} \qquad (15)$$

Where V_1 is voltage across capacitor. The voltage transfer gain (G) is:

$$G = \frac{V_0}{V_{in}} = \left(\frac{4-2k}{1-k} \right) \qquad (16)$$

4. PI Controller based Converter

The traditional Proportional Integral controller is a simple method and is extensively utilized in various applications. PI controller raises the reaction speed. It creates minute level of steady state error. In this study voltage error is given as input to PI control system and response is accepted as the duty ratio of the switch in the converter.

General equation of PI controller is given below

$$U(s) = K_p E(s) + \frac{K_i}{s} E(s) \qquad (17)$$

where proportional constant is K_p, the integral gain is K_i, controller input and the controller output is given as E(s) and U(s). The optimal values of K_p & K_i are found by using Ziegler-Nichols' technique. But this control system produces high overshoot and voltage ripple.

5. Converter Control Using Fuzzy Logic Controller

The numerical method for handling the inexact data and bugs that have numerous keys instead of one is the Fuzzy logic controller (FLC). In FLC non integer, Linguistic, variables are utilized, making it similar to the way humans think. Fuzzy control method is an efficient way for handling the instabilities and unpredictability relating to vagueness (Leyva et al., 1997). In this study, FLC is employed to control overshoot.

Fuzzy inference system is the full title for the scheme which utilizes fuzzy reasoning for mapping an input space into an output space. Numerous methods describe the outcome of this procedure; this study implements the max-min technique of inference. Voltage error (*e*) and change in error (ec) are the two inputs of Mamdani-type fuzzy controller. FLC produces duty ratio as output.

$$e_v = V^* - V_o \qquad (18)$$

In (18) V^* is the reference voltage. NB - negative big, NS - negative small, Z - zero, PS -positive small and PB - positive big are the five membership functions of output and both inputs. The analytical method for

converting fuzzy values into crisp values is stated as defuzzification. Among various types of defuzzification methods, centroid method of defuzzification is used in this study. Fuzzy rules of D are illustrated in Table 1. Figure 2(a) shows the input membership functions, Figure 2(b) shows the Output membership functions of D (Ofoli & Rubaai, 2006).
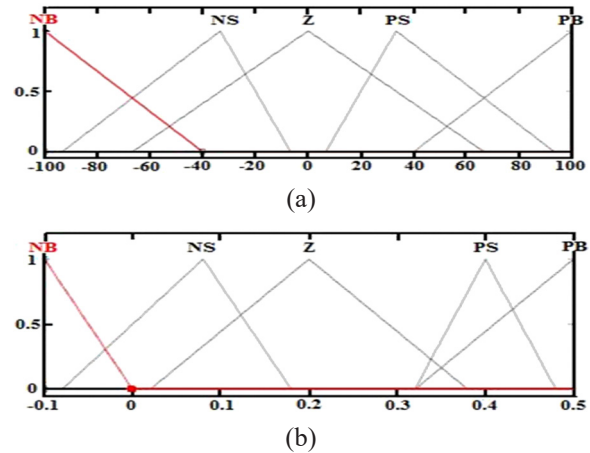

(a)

(b)

Figure 2. (a). Membership functions of input e & ec, (b) Output Membership functions of D

Table 1. Fuzzy Rules of D

ec \ e	NB	NS	Z	PS	PB
NB	NB	NS	NS	Z	PS
NS	NB	NS	NS	PS	PB
Z	NB	NS	Z	PS	PB
PS	NB	NS	PS	PS	PB
PB	NS	Z	PS	PS	PB

6. Report of Artificial Neural Network

Artificial Neural Networks are computational models, their process is based on parallel processing. Weights are one of the internal parameters of the processing parameters. Any dynamic, linear or non-linear, actions of transmission in the network can be practically performed by varying the weights (Ofoli & Rubaai, 2006).

By assuming these characteristics, the neural networks can also be used as a control system for switch-mode systems. The back-propagation algorithm, delta learning rule, Hoffman adaptive neural scheme, wizhai training technique and self-organizing map were used for the intended DC

to DC converter for implementing the Artificial Neural Network Controller.

Edifying the Neurons

The linear structure is implemented in ANN control system. The ANN controller does the following steps (Beale et al., 2010):

- The scalar input 'p' is multiplied with the weight. Thus, for every feedback cycle, the input will increase;

- The delay unit holds up the computed data for a specified period of time. By the multiplexer, the data hold-up is created in the delay unit, then the processed input is multiplexed again;

- The holdup input is added with the scalar bias. The output of the dot product unit is also multiplexed;

- The total network addition of the response (z) is fed to the saturation unit, for checking if the linearized output attains the saturation condition;

- The scalar variable 'p' is once again computed with the acquired output. So that the output is precise corrected and gets increased for every feedback cycle. Thus, the ANN controller produces the output;

- The ANN control system response is relationally compared with the reputational series pulses;

- The gate signal for S_2. is provided based on the compared response. The gate signal for S_1 is given based on compared response and based on inverted response (z).
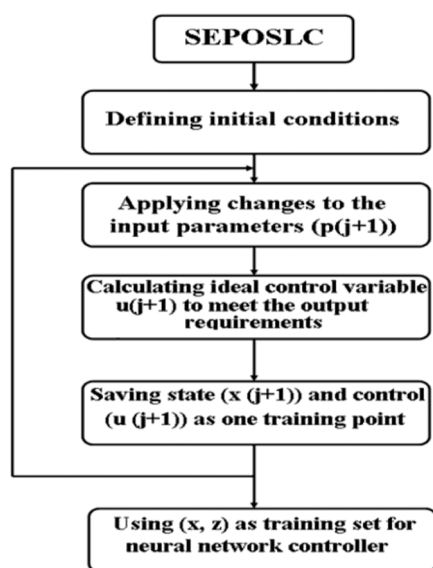

Figure 3. Flow chart of artificial neural network controller

The inputs provided for ANN controller are exact response voltage acquired by the SEPOSLC and rate-limited reference voltage. By multiplexing the two inputs, the ANN controller gets the selected input. Flow diagram of ANN controller is shown in Figure 3.

7. ANN with SMC for Converter Control

In order to control the duty ratio of the converter the sliding surface is attained. In a conventional sliding mode controller, the voltage error is X_1, X_2 is the amount of change in voltage error, X_3 is the addition of voltage error. The switching function adopted General SM control law as follows

U=1 when S>0

U=0 when S<0

$$U = \frac{1}{2(1+\text{sgn}(S))} \qquad (19)$$

S is the instant state variable's path which is depicted below

$$S = m_1 X_1 + m_2 X_2 + m_3 X_3 \qquad (20)$$

where m_1, m_2 and m_3 are sliding coefficients. By enforcing S to 0 sliding surface is attained. To minimize these computations in this paper simplified SMC is analyzed. The duty ratio tuned by the ANN is applied to this controller, and the sliding surface enforces converter to produce the required voltage.

$$S_v = e_v + K_v \int e_v \, dt \qquad (21)$$

In equation (21) e_v is the voltage error and K_v is the controller design constant.

Since the output of ANN is again fine-tuned using SMC, the ANN-SMC controller attains improved performance compared to all other controllers.

8. SEPOSLC with Inverter Fed BLDC Motor

For analyzing the nonlinear load in an SEPOSLC converter, three-phase inverter fed BLDC motor is proposed. Three-phase insulated-gate bipolar transistor (IGBT) inverter is supplied from the converter, and it is controlled by using Hall Effect sensor, decoder signal from BLDC motor. The

controlled voltage from the converter enhances the performance of motor and reduces the steady-state error.

9. Simulation Results of SEPOSLC Converter

Matlab/Simulink model is developed to analyze various controllers based SEPOSLC Converter powered three-phase BLDC motor. The simulation model is developed with an adjustable voltage supply. The response voltage is feedback to voltage controller. The response of control system is compared with a saw-like carrier wave and produced signals are fed to the switches in the converter.

Input Variance in SEPOSLC Converter

The input voltage varies from 6V - 12V to analyze the performance of various controllers proposed. The response voltage from the systematic outcome of SEPOSLC converter for input of 14V using PI, FLC, ANN, ANN with SMC is shown in Figure 4.

From Figure 4(a), it can be noticed that PI controller in converter control produces a voltage which is close to the reference value. But it produces high overshoot as well as ripple in voltage in the response voltage. Overshoot at the output is referred as overvoltage to load produced due to the poor control of converter. Voltage ripple makes the voltage to the load oscillate which reduces performance and life of load.

From Figure 4(b), it is obvious that fuzzy controller in converter control eliminates overshoot. Elimination of overshoot avoids excess voltage to the load, but voltage ripple produced by FLC controlled converter is yet to be reduced.

From Figure 4(c), one can notice effectiveness of artificial intelligent ANN controller in converter control. ANN eliminates overshoot and reduces voltage ripple effectively compared to PI and FLC. But the range of voltage ripple is 1.2% which is very low compared to the 2.1% and 4.4% of ripple produced by PI and FLC respectively. Even though the voltage ripple is low, this will lead to ripple in the inverter voltage and results in oscillation in the speed of BLDC motor.
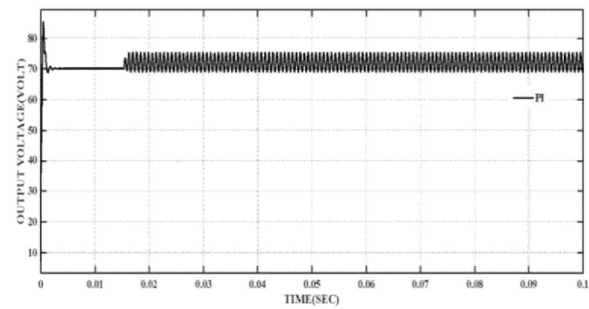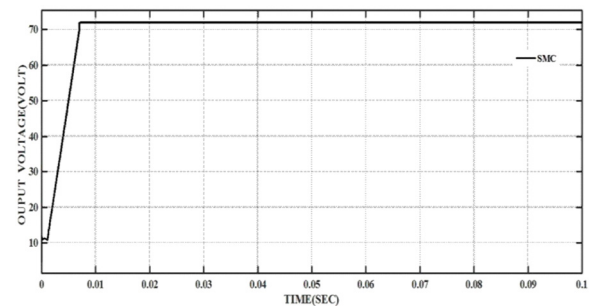

(a)
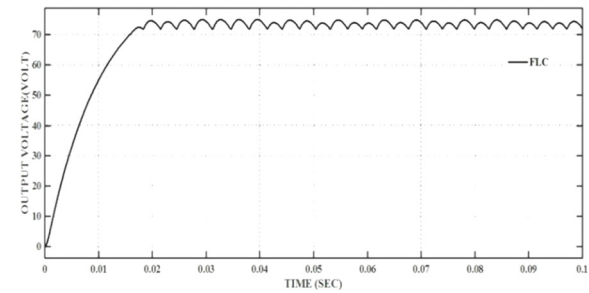
(b)
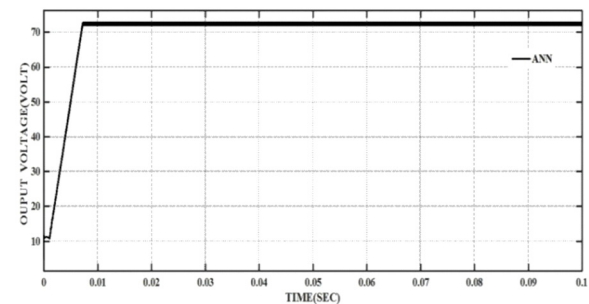
(c)

(d)

Figure 4. Performance of SEPOSLC converter at 14V input, (a) Performance of PI, (b) Performance of FLC, (c) Performance of ANN, (d) Performance of ANN-SMC

From Figure 4(d), one can notice that proposed ANN with SMC controller eliminates overshoot and reduces the voltage ripple to 0.029%. In comparison with the conventional PI controller almost 99% of voltage ripple is reduced by the

proposed ANN with SMC controller. It results in the elimination of overvoltage and oscillation in the speed of motor connected with the converter-fed drive. This is the required property of the converter for running the inverter-fed motor.

From Table 2, it can be noticed that only PI produces overshoot in voltage. FLC eliminates overshoot, but voltage ripple is high. ANN controller also eliminates overshoot, and it minimizes the voltage ripple. ANN SMC control system provides higher throughput in comparison with all other control systems with regard to peak overshoot, voltage ripple and settling time. Hence ANN SMC controller which attains best performance is executed in hardware for experimental analysis.

Table 2. Trade-off of various controllers on SEPOSLC converter

Controllers	Peak overshoot (%)	Voltage ripple (%)	Settling time (sec)
PI	18.35	2.1	0.004
FLC	0	4.4	0.0183
ANN	0	1.223	0.0072
ANN-SMC	0	0.02916	0.006996

10. Hardware Output of SEPOSLC Converter
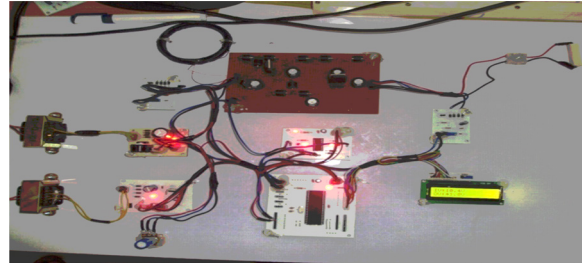
Experimental Setup of the Intended System

The converter is designed to produce 12V output with various loads. Table 3 includes the hardware requirements for the intended system.

Table 3. Hardware specifications

| S. No	Requirements	Device or Software
1	Embedded Controller	PIC16F887
2	Coding	Embedded C Language
3	C compiler	HITECH C
4	Simulator	MPLAB Simulator
5	Programmer	PIC KIT3 Programmer
6	Schematic Software (Circuit Designing)	Express Schematic
7	Printed Circuit Board (PCB) Designing	Express PCB

Experimental Setup for the Proposed System with Resistive Load

For a linear load analysis ANN with SMC-controlled SEPOSLC converter is analyzed with resistive load of 50 Ω. Figure 5 shows the experimental setup of SMC-controlled SEPOSLC with resistive load.
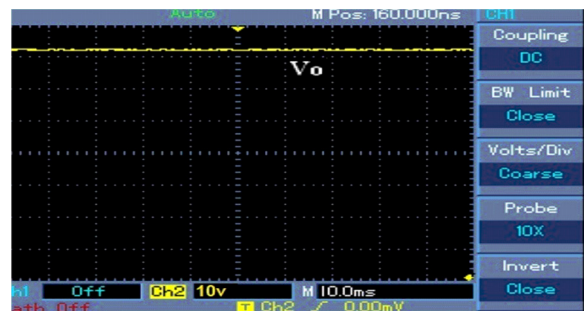

Figure 5. Experimental setup of Intended System with resistive load

For an analysis of ANN with SMC variable input voltage 6V to 11V is given to the SEPOSLC to produce 12V output. The input and response voltage of intended system along with resistive load are shown in Figure 6.
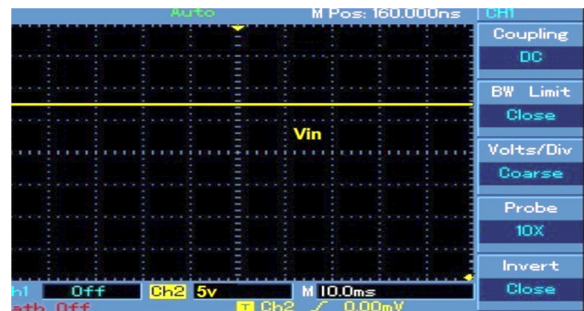
(a)

(b)

Figure 6. Performance of SEPOSLC converter using ANN with SMC for 8V input with resistive load (a) Input voltage of SEPOSLC at 8V (b) Output voltage of SEPOSLC at 8V input

In Figure 6 it can be noticed that the input to the converter is increased to 12V in SEPOSLC converter. The smooth response voltage of converter shows the effectiveness of ANN with SMC.

Experimental Setup for the Proposed System with BLDC Motor Load

For an analysis of proposed system with the nonlinear load, SEPOSLC is proposed with the load of three-phase inverter-fed BLDC motor. 12V, 3-phase BLDC motor is considered as load. Figure 7 shows the hardware of SEPOSLC converter using ANN with SMC control system with BLDC motor load.
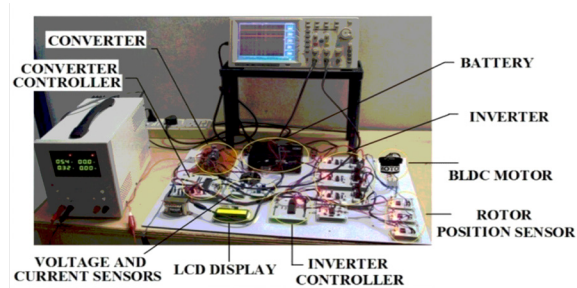

Figure 7. Hardware system with BLDC motor load

In comparison with hardware setup from Figure 5, in Figure 7, resistive load is replaced by a BLDC motor. Three-phase inverter circuit is introduced after a converter to feed AC supply to the motor. For an analysis ANN with SMC controller input voltage is varied for SEPOSLC converter.

Figure 8(a) shows the outcome of SEPOSLC converter using ANN with SMC for 8V input. The orange color wave represents the input voltage while the yellow wave is the output voltage. For 8V input, it produces 12V output. Figure 8(b) shows the pulse produced by the ANN-SMC controlled duty ratio for SEPOSLC converter. Figure 8(a) shows the effect of this control in output voltage control. The response of SEPOSLC converter using ANN with SMC for 11V input is shown in Figure 8(c). For 11V input, it produces 12V output.
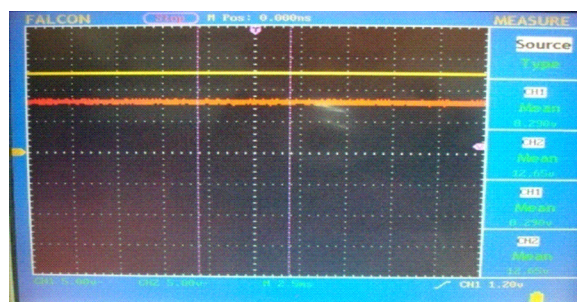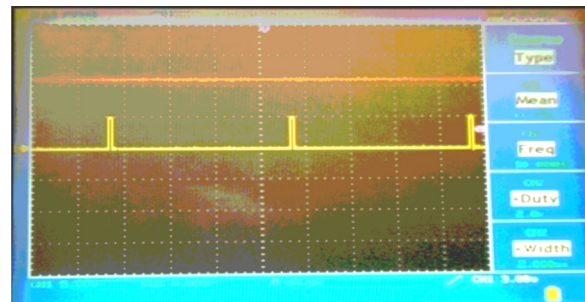

(a)
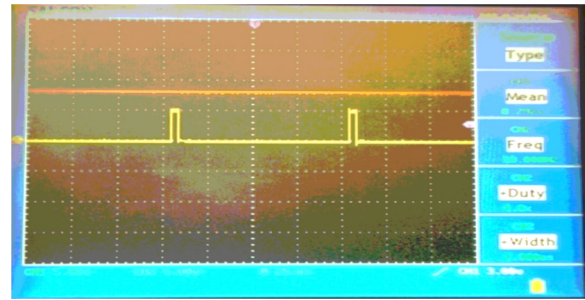
(b)
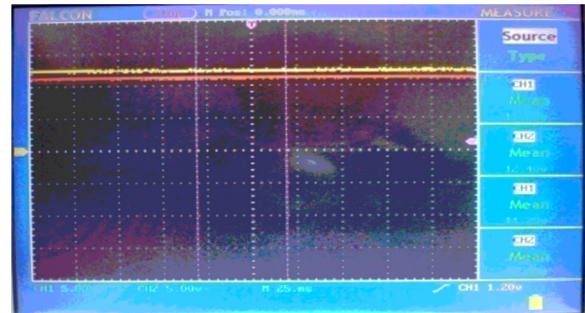
(c)

(d)

Figure 8. (a) Response of ANN-SMC controlled converter at 8V input, (b) Duty ratio controlled by ANN SMC controller at 8V input, (c) Response of ANN -controlled converter at 11V input, (d) Duty ratio controlled by ANN SLC converter at 11V input

Figure 8(d) shows the pulse width modulated (PWM) output produced by the ANN-SMC controller for SEPOSLC converter at the 11V input. Figure 8(c) shows the effect of this control in response voltage control. It is obvious that the pulse width in Figure 8(d), is lower than in Figure 8(b). In the case of Figure 8(b) input voltage is 8V, so the pulse width is large compared to pulse width in Figure 8(d) at 11V input voltage.

From Figures 8(a) and (c) one can notice the performance of ANN controlled converter at 8v and 11V inputs respectively, the converter gives constant 12V output if the input is either 8V or 12V.

Figures 8(b) and (d) show the pulse produced by ANN-SMC controlled duty ratio for the input of 8v and 11V respectively. ANN-SMC controlled SEPOSLC varies pulse width or duty ratio based on the input voltage. Hence a change in duty ratio with respect to change in input voltage results in constant output voltage as it is shown in Figures 8(a) and (c). This controlled voltage is fed to three- phase inverter for supplying BLDC motor. Speed status of BLDC motor using ANN-SMC controlled SEPOSLC is shown in Figure 9.
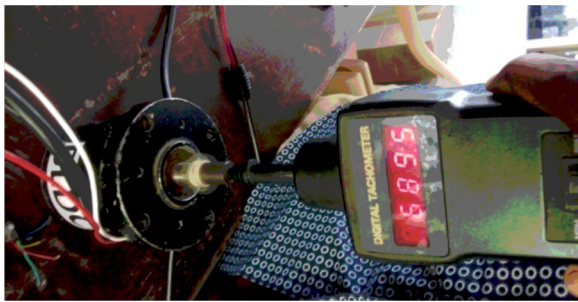
Figure 9. Speed status of BLDC motor using ANN-SMC controlled SEPOSLC

Effectiveness of the System in Hardware

The formula for calculating the effectiveness of the previously illustrated positive output super lift converter is

$$\text{Efficiency}\eta = \frac{\text{output power}}{\text{input power}} * 100\% \qquad (22)$$

$$\text{Efficiency}\eta = \frac{\text{input power}(PE) - \text{losses}(EL)}{\text{input power}(PE)} * 100\% \qquad (23)$$

$$\text{Efficiency}\eta = 70.81\%$$

The acquired effectiveness is low, and the remaining 29.19% of effectiveness is due to the usage of numerous passive components like one inductor, five capacitor, two MOSFET switches and nine diodes. The overall power loss due to these passive elements is calculated by using the formula below.

Total power loss

$$= W_{L1} + W_{c1} + W_{c2} + W_{c3}$$
$$+ W_{c4} + W_{c5} + W_{sw1} + W_{sw2} \qquad (24)$$
$$+ W_{D1\ to\ D9}$$

Total power loss = 29.19 W

Technical Specification

Table 4 illustrates the essential parameters and their corresponding values for the SEPOSLC converter.

Table 4. Parameter list of SEPOSLC converter

Parameter list	Symbol	Value
Input Voltage	V_{in}	6V
Output Voltage	V_o	12V
Inductor	L_1	100µF
Capacitor	$C_1 - C_5$	30µF
Nominal Switching Frequency	f_s	100kHz
Load Resistance	R_0	50Ω
Range of Duty Cycle	k	0.3 to 0.9
Desired Duty Cycle	k	0.5

11. Conclusion

In this paper, SEPOSLC converter is analyzed in Matlab simulation by using different control systems such as PI, fuzzy logic controller and ANN controller. The throughput of all controllers is compared with the proposed ANN-SMC controller. ANN-SMC controller is proposed in this analysis with a view of reducing voltage ripple and peak overshoot in response voltage. In the framework of this systematic analysis, FLC in converter control system diminishes overshoot but increases the voltage ripple as compared to PI controller, whereas ANN-controlled converter produces no overshoot but generates voltage ripple in the range of 1.2% which has to be reduced. Proposed ANN with SMC controller attains satisfactory performance in all aspects compared to all other analyzed controllers.

Experimental analysis of proposed system with resistive load and BLDC motor load shows its effectiveness for a proposed system with linear and nonlinear load. The output voltage of converter is smooth and constant in both cases of loads such as resistive load and three-phase inverter-fed BLDC motor load. From the experimental analysis it can be noticed that the throughput results of the proposed ANN-SMC controlled converter are similar to simulation results. The usage of ANN-SMC control system could be a better choice in a situation that requires exceptional regulation characteristics and excellent dynamical output specifications.

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