Real Time Analysis of Positive Output Super Lift Converter Using ANN Controller

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Abstract: The Artificial neural network controller is used for controlling any electrical and electronic system using the logical method. The controller performs the logical function by utilizing the unique learning algorithms. The application of artificial neural network controller in positive output super lift converter enables the system to maintain the stability, reliability, and performance during the input-output parameterization. The hardware and simulation works are carried out in this proposed model. The comparative study with existing controller models is impacted. In all such cases, the ability of the super lift converter system using artificial neural network controller yields the best in class performance, stability and efficiency for both line and load variation.

Keywords: stability of super lift converter, hardware efficiency of super lift converter, a performance comparison of the converter, comparative study on converters.

1. Introduction

Intelligent control is a class of control techniques that use the various artificial intelligence of computing approaches like neural networks, fuzzy logic, machine learning, evolutionary computation and genetic algorithm. Artificial neural networks are a family of the model developed using machine learning [3,7]. This ANN is used to determine the approximate functions for larger inputs [4,9]. ANN is the system of interconnected neurons which exchanges the information with neighboring neurons.

The each neuron in the ANN possesses numeric weights which are tuned to the desired value using various learning methods [2]. The inputs are modulated in ANN based on these neurons numeric value and yields the corresponding output. This sort of ANN system performs as a controller for any application system [13].

The voltage level of a Direct Current (DC) can be converted from one voltage level to another voltage level by a power electronic circuit called DC to DC converter [5]. The DC to DC converter generates the DC output voltage for the given DC input voltage. The essential requirements for a good DC to DC converter are to provide a high voltage transfer gain, to reduce the occurrence of Alternating Current (AC) ripple voltage in the DC output voltage, to provide good isolation between the input source and load, and to regulate the output DC voltage from line and load variation efficiently.

A new series of DC to DC converter which satisfies all the essential requirements of DC to DC converter is Positive Output Super Lift converter (POSLC). This converter implies the voltage lift technique which produces the positive to positive voltage conversion with a higher proportion of voltage transfer gain.

Theoretically, the elementary DC to DC converters can achieve a high step up voltage transfer gain with an extremely high duty cycle. Unfortunately, in practice, the step-up voltage gain is limited because of the effect of power switches, rectifier diodes, and the Equivalent Series Resistance (ESR) of inductors and capacitors which account for heavy conduction losses. Moreover, the extremely high duty cycle operation will result in a serious reverse recovery problem.

Each functional cell of the super lift converters utilizes the Voltage Lift (VL) technique, which is an efficient method widely applied in electronic circuit design, to realize the performance improvement. In this converter voltage unit cells in cascade connection and the transformerless single-switch operation are successfully implemented to provide a very high step up voltage transfer gains. Super lift technique has been developed which performs the output voltage increasing stage by stage along in geometric progression.

In a design and implementation solution, the analysis on their mathematical modeling and control strategies is necessary to promote the practical applications of super lift DC to DC converter. The derived Transfer function for the split capacitor type elementary additional series positive output super lift converter helps to control and maintain the stability of the system. The Artificial Neural Network Controller (ANNC) is designed for controlling the SEPOSLC converter. The neurons in ANNC are trained by utilizing the values of transfer function [9,12]. The neurons are trained up by an online learning algorithm. The design of artificial neural network controller benefits the SEPOSLC converter with a high line and load variation robustness and high stability.

2. Operation of SEPOSLC Converter

2.1 Description of the circuit diagram

Figure 1 represents the circuit diagram of SEPOSLC converter, which possesses both the active and passive elements. The DC power supply V_{in} is the active voltage source for the SEPOSLC converter. The passive elements of the SEPOSLC converter are the resistor R_0, capacitor C_1, C_2, C_3, C_4, C_5, and inductor L_1. The SEPOSLC circuit also consists of a power switching element which is n-channel MOSFET switch and freewheeling diodes for forwarding the current during DC bias.

There is two n-channel MOSFET switch present in the SEPOSLC converter; they are a switch S_1 and S_2. The resistor R_0 in the converter circuit is considered to be a load resistance. There are nine diodes occurred in the circuit; they are D_1, D_2, D_3, D_4, D_5, D_6, D_7, D_8, D_9 respectively. The diodes in the converter circuit help to forward the current accurately during the switching condition.

The split capacitor type elementary additional series positive output super lift converter assumed to be in an ideal state and continuous condition mode. The converter circuit undergoes two switching modes [6]. The mode 1 of SEPOSLC converter is attained when the switch S_1 is closed and S_2 is open. The mode 2 of SEPOSLC converter is achieved when the switch S_1 is open and S_2 is closed. The circuit diagram for both the modes of SEPOSLC converter is described. The state space representation of the SEPOSLC circuit is derived for both the mode 1 (ON state) and mode 2 (OFF state).

The state space matrix representation of the entire split capacitor type elementary additional series positive output super lift converter circuit is obtained by adding ON state space matrix with (1-k) of OFF state space matrix. The transfer function is derived from the SEPOSLC state matrix using state space to transfer function conversion formula in MATLAB software. The Bode plot and root locus describe the stability of the derived transfer function. The general coding prescribed for state space to transfer function conversion is as given below.

$$[b,a] = \text{sstotf}(A,B,C,D) \quad (1)$$

2.2 Description of MODE 1 (ON State) circuit diagram

Figure 2 represents the circuit diagram of SEPOSLC converter under mode 1. When the input voltage V_{in} has applied the capacitors, C_1 and C_2 are charged to attain the steady state

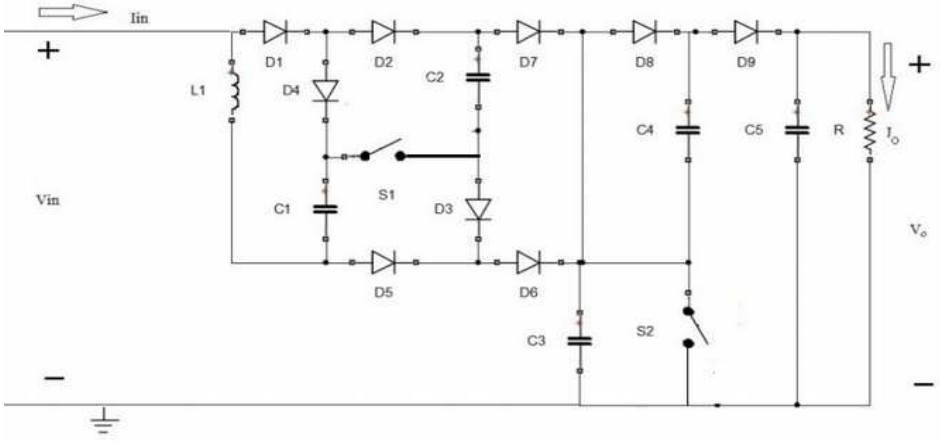

Figure 1. Circuit diagram of split capacitor type elementary additional series positive output super lift converter.

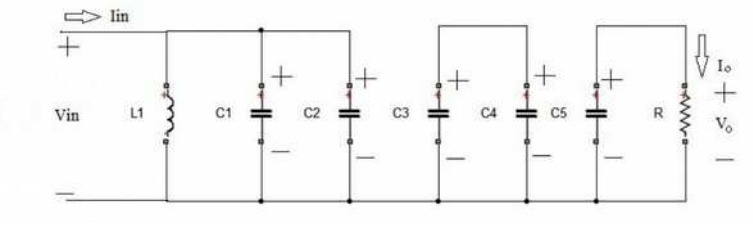

Figure 2. Circuit diagram of mode 1 (ON state) of SEPOSLC converter.

condition. During this mode, the current passing through the inductor L_1 increases when V_{in} is applied. The switching period for mode 1 (ON state) is kT [1].

The state space representation for the mode 1 of split capacitor type elementary additional series positive output super lift converter is derived with the help of electrical circuit analysis. The state space matrix formed for the mode 1 circuit is the 6×6 matrix as there are six passive elements present in the circuit. The state space matrix is formed from state matrix (A), input matrix (B), output matrix (C) and feedback matrix (D). The general formula for representing state space matrix is given below

$$S[X] = A[X] + B[U] \tag{2}$$

$$Y[X] = C[X] + D[U] \tag{3}$$

The state space matrix for the mode 1 SEPOSLC circuit is given in eqs. (4) and (5).

2.3 Description of MODE 2 (OFF State) circuit diagram

Figure 3 represents the circuit diagram of SEPOSLC converter under mode two conditions. When the input voltage V_{in} has applied the capacitors, C_1 and C_4 are charged to

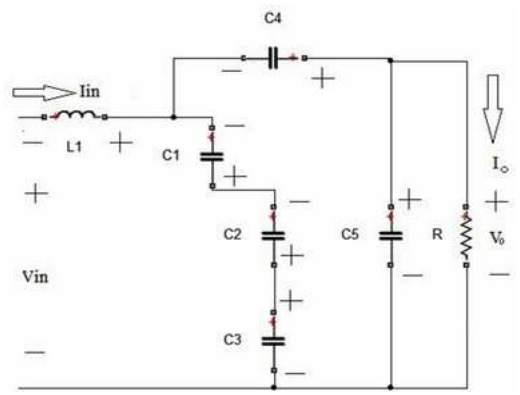

Figure 3. Circuit diagram of mode 2 (OFF state) of SEPOSLC converter.

$$\frac{d}{dt}\begin{pmatrix} i_{L_1} \\ V_{C_1} \\ V_{C_2} \\ V_{C_3} \\ V_{C_4} \\ V_{C_5} \end{pmatrix} = \begin{pmatrix} 0 & \frac{-1}{L_1} & 0 & 0 & 0 & 0 \\ -\frac{1}{C_2} & 0 & -\frac{C_2}{C_1} & 0 & 0 & 0 \\ -\frac{1}{C_2} & -\frac{C_1}{C_2} & 0 & -\frac{C_3}{C_2} & 0 & 0 \\ \frac{1}{C_3} & \frac{C_1}{C_3} & \frac{C_2}{C_3} & 0 & -\frac{C_4}{C_3} & 0 \\ \frac{1}{C_4} & \frac{C_1}{C_4} & \frac{C_2}{C_4} & \frac{C_3}{C_4} & 0 & \frac{C_5}{C_4} \\ \frac{1}{C_5} & \frac{C_1}{C_5} & \frac{C_2}{C_5} & \frac{C_3}{C_5} & \frac{C_4}{C_5} & 0 \end{pmatrix} \begin{pmatrix} i_{L_1} \\ V_1 \\ V_2 \\ V_3 \\ V_4 \\ V_5 \end{pmatrix} + \begin{pmatrix} 1/L_1 \\ \frac{1}{R_{in} C_1} \\ \frac{1}{R_{in} C_2} \\ 0 \\ 0 \\ 0 \end{pmatrix} (V_{in}) \tag{4}$$

$$\frac{d}{dt}\begin{pmatrix} i_{L_1} \\ V_{C_1} \\ V_{C_2} \\ V_{C_3} \\ V_{C_4} \\ V_{C_5} \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 & 0 & 0 & \frac{1}{R_0 C_5} \end{pmatrix} \begin{pmatrix} i_{L_1} \\ V_1 \\ V_2 \\ V_3 \\ V_4 \\ V_5 \end{pmatrix} + (1)(V_{in}) \tag{5}$$

attain the steady state condition. During this mode, the current passing through the inductor L_1 decreases when V_{in} is applied. The switching period for mode 2 (OFF state) is (1- kT).

The state space representation for the mode 2 of split capacitor type elementary additional series positive output super lift converter is derived with the help of electrical circuit analysis. The state space matrix formed for the

mode 2 circuit is of 6×6 matrix as there are six passive elements present in the circuit [8]. The state space matrix is formed from state matrix (A), input matrix (B), output matrix (C) and feedback matrix (D).

The state space matrix for the mode 2 SEPOSLC circuit is given in eqs. (6) and (7).

inductor L_1 and capacitor C_1-C_5 are expressed in eqs. (11) and (12).

$$C_5=\frac{(1-k)V_0}{f*\Delta V_0*R} \tag{11}$$

$$L=\frac{V_{\text{in}}.k.T}{\Delta IL} \tag{12}$$

$$\frac{d}{dt}\begin{pmatrix} i_{L_1} \\ V_{C_1} \\ V_{C_2} \\ V_{C_3} \\ V_{C_4} \\ V_{C_5} \end{pmatrix}=\begin{pmatrix} 0 & \frac{-1}{L_1} & 0 & 0 & 0 & 0 \\ \frac{1}{C_2} & 0 & 0 & 0 & -\frac{C_4}{C_1} & 0 \\ \frac{1}{C_2} & \frac{C_1}{C_2} & 0 & -\frac{C_3}{C_2} & 0 & 0 \\ \frac{1}{C_3} & \frac{C_1}{C_3} & \frac{C_2}{C_3} & 0 & -\frac{C_4}{C_3} & 0 \\ \frac{1}{C_4} & \frac{C_1}{C_4} & \frac{C_2}{C_4} & \frac{C_3}{C_4} & 0 & -\frac{C_5}{C_4} \\ \frac{1}{C_5} & \frac{C_1}{C_5} & \frac{C_2}{C_5} & \frac{C_3}{C_5} & \frac{C_4}{C_5} & 0 \end{pmatrix}\begin{pmatrix} i_{L_1} \\ V_1 \\ V_2 \\ V_3 \\ V_4 \\ V_5 \end{pmatrix}+\begin{pmatrix} 1/L_1 \\ \frac{1}{R_{\text{in}}C_1} \\ \frac{1}{R_{\text{in}}C_2} \\ \frac{1}{R_{\text{in}}C_3} \\ \frac{1}{R_{\text{in}}C_4} \\ 0 \end{pmatrix}(V_{\text{in}}) \tag{6}$$

$$\frac{d}{dt}\begin{pmatrix} i_{L_1} \\ V_{C_1} \\ V_{C_2} \\ V_{C_3} \\ V_{C_4} \\ V_{C_5} \end{pmatrix}=\begin{pmatrix} 0 & 0 & 0 & 0 & 0 & \frac{1}{R_0C_5} \end{pmatrix}\begin{pmatrix} i_{L_1} \\ V_1 \\ V_2 \\ V_3 \\ V_4 \\ V_5 \end{pmatrix}+(1)(V_{\text{in}}) \tag{7}$$

2.4 Derivations of the transfer function of SEPOSLC converter

The overall state space representation of the split capacitor type elementary additional series positive output super lift converter is given in eqs. (8), (9) and (10).

$$T(S)=\text{ON state matrix}+(1-k)\text{OFF state matrix} \tag{8}$$

$$\frac{d}{dt}\begin{pmatrix} i_{L_1} \\ V_{C_1} \\ V_{C_2} \\ V_{C_3} \\ V_{C_4} \\ V_{C_5} \end{pmatrix}=\begin{pmatrix} 0 & 0 & 0 & 0 & 0 & \frac{1+(1-k)}{2R_0C_5} \end{pmatrix}\begin{pmatrix} i_{L_1} \\ V_1 \\ V_2 \\ V_3 \\ V_4 \\ V_5 \end{pmatrix}+(1)(V_{\text{in}}) \tag{10}$$

The state matrix and the output matrix of the overall SEPOSLC circuit is an addition of ON state matrix with (1-k) of OFF state matrix. The transfer function of the split capacitor type elementary additional series positive output super lift converter i obtained by subjecting the values of resistor R_0(50Ω), capacitor C_1, C_2, C_3, C_4, C_5, the value of each capacitor is each (30μF) and inductor L_1(100μH). The design of

Thus the obtained transfer function is given in eq. (13).

It is known that the inductor current decreases during switch OFF state and increases during switch ON state; therefore the peak to peak inductor ripple current and voltage transfer gain is given by the following equations:

$$\Delta iL=\frac{V_{\text{in}}}{L}kT=\frac{V_0-V_1-V_{\text{in}}}{L}(1-k)T \tag{14}$$

$$V_0=\left(\frac{1}{1-k}+\frac{3-2k}{1-k}\right)V_{\text{in}} \tag{15}$$

The voltage transfer gain is given in eq. (16).

$$G=\frac{V_0}{V_{\text{in}}}=\left(\frac{1}{1-k}+\frac{3-2k}{1-k}\right) \tag{16}$$

3. Stability Analysis for the Transfer Function

3.1 Bode plot for the transfer function of SEPOSLC converter

Figure 4 represents the Bode plot of the obtained transfer function in a closed loop. This bode plot infers about the phase margin, gain margin, peak gain for the open loop SEPOSLC converter and it also estimated the stable closed loop response of SEPOSLC [14]. Thus the Bode plot infers that the obtained transfer function is stable.

$$\frac{d}{dt}\begin{pmatrix} i_{L_1} \\ V_{C_1} \\ V_{C_2} \\ V_{C_3} \\ V_{C_4} \\ V_{C_5} \end{pmatrix} =$$

$$= \begin{pmatrix} 0 & \frac{-1}{L_1} & 0 & 0 & 0 & 0 \\ -\frac{1}{C_2}+\frac{(1-k)}{C_1} & 0 & \frac{-C_2}{C_1} & 0 & -\frac{C_4(1-k)}{C_1} & 0 \\ -\frac{1}{C_2}+\frac{(1-k)}{C_2} & -\frac{C_1}{C_2}+\frac{C_1(1-k)}{C_2} & 0 & -\frac{C_3}{C_2}-\frac{C_3(1-k)}{C_2} & 0 & 0 \\ \frac{1}{C_3}+\frac{(1-k)}{C_3} & \frac{C_1}{C_3}+\frac{C_1(1-k)}{C_3} & \frac{C_2}{C_3}+\frac{C_2(1-k)}{C_3} & 0 & -\frac{C_4}{C_3}-\frac{C_4(1-k)}{C_3} & 0 \\ \frac{1}{C_4}+\frac{(1-k)}{C_4} & \frac{C_1}{C_4}+\frac{C_1(1-k)}{C_4} & \frac{C_2}{C_4}+\frac{C_2(1-k)}{C_4} & \frac{C_3}{C_4}-\frac{C_3(1-k)}{C_4} & 0 & -\frac{C_5}{C_4}+\frac{C_4(1-k)}{C_5} \\ \frac{1}{C_5}+\frac{(1-k)}{C_5} & \frac{C_1}{C_5}+\frac{C_1(1-k)}{C_5} & \frac{C_2}{C_5}+\frac{C_2(1-k)}{C_5} & \frac{C_3}{C_5}-\frac{C_3(1-k)}{C_5} & \frac{C_4}{C_5}+\frac{C_4(1-k)}{C_5} & 0 \end{pmatrix} \begin{pmatrix} i_{L_1} \\ V_1 \\ V_2 \\ V_3 \\ V_4 \\ V_5 \end{pmatrix} + \tag{9}$$

$$+ \begin{pmatrix} 1/L_1+\frac{1-k}{L_1} \\ \frac{1}{R_{\text{in}}C_1}+\frac{1-k}{R_{\text{in}}C_1} \\ \frac{1}{R_{\text{in}}C_2}+\frac{1-k}{R_{\text{in}}C_2} \\ \frac{1-k}{R_{\text{in}}C_3} \\ \frac{1-k}{R_{\text{in}}C_4} \\ 0 \end{pmatrix} (V_{\text{in}})$$

$$T(s) = \frac{3.704\text{e}17\, s^2 + 1.235\text{e}22\, s + 2.877\text{e}11}{s^6 + 1.693\text{e}09\, s^5 + 5.789\text{e}10\, s^4 + 2.483\text{e}15\, s^3 + 8.029\text{e}19\, s^2 + 1.235\text{e}22\, s} \tag{13}$$

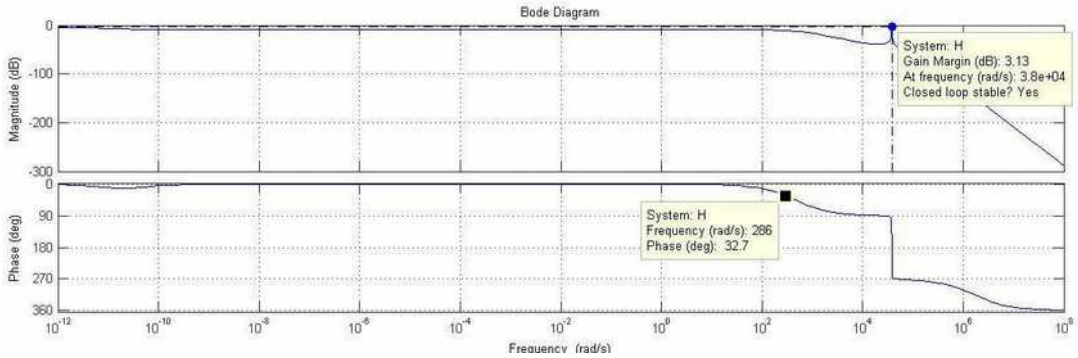

Figure 4. Bode plot for the transfer function of SEPOSLC converter.

3.2 Root locus for the transfer function of SEPOSLC converter

Figure 5 represents the root locus of the obtained transfer function. The root locus denotes the impulse response of the received transfer function [11]. Where the obtained poles of the impulse response lie in the left plane of the root locus and ensure that the system is absolutely stable. Thus the root locus plot infers that the obtained transfer function is stable.

3.3 Signal flow graph method

The Figure 6 represents the signal flow graph for the overall state space matrix of the SEPOSLC system. The obtained transfer function is cross verified using Mason's Gain Formula by reducing the state space variables in signal flow graph node representation. Hence the transfer function obtained for the ANNC controlled SEPOSLC using both the methods are same and relevant.

The obtained transfer function using signal flow graph analysis is cross verified by finding the equivalent temporary value and second order system values for the subjected super lift converter. It makes use of Eigenvalue, damping frequency, Zeros and Poles of the obtained transfer function for the proposed super lift converter. Thus the calculated 'temp' value matches the coefficient of s^2. It is illustrated below.

3.4 Routh Hurwitz criteria

The stability analysis of the proposed converter using the neural network is executed by calculating the poles of the system using Routh-Hurwitz criteria. It is explained below

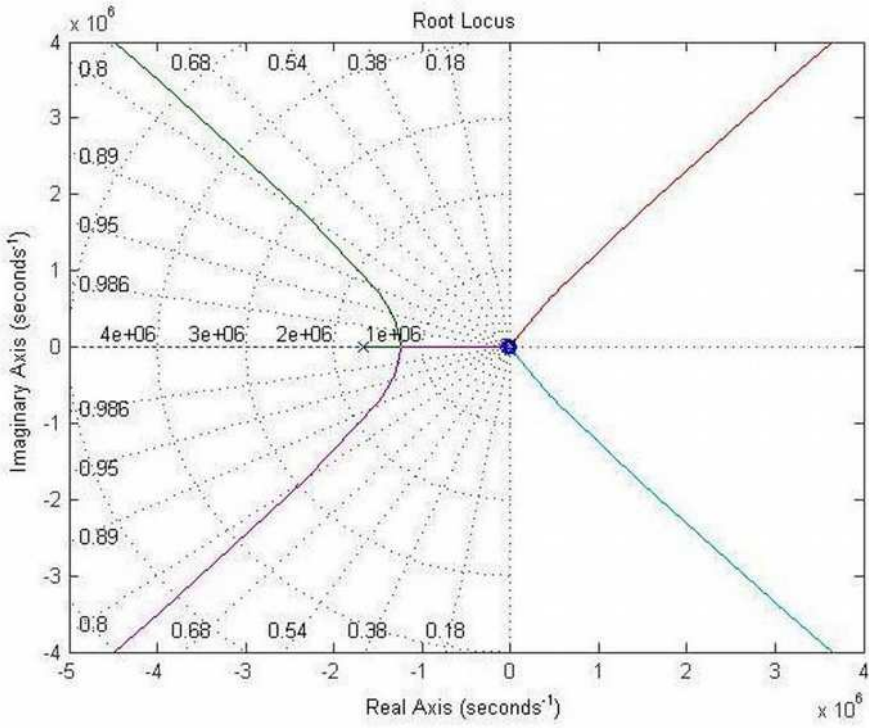

Figure 5. Root locus of the transfer function of SEPOSLC converter.

$$T(s)=\frac{3.704\text{e}17\,s^2+1.235\text{e}22\,s+2.877\text{e}11}{s^6+1.693\text{e}09\,s^5+5.789\text{e}10\,s^4+2.483\text{e}15\,s^3+8.029\text{e}19\,s^2+1.235\text{e}22\,s+0.665\text{e}24} \tag{17}$$

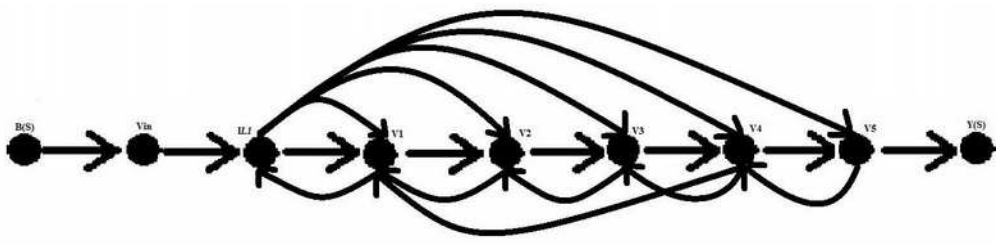

Figure 6. Signal Flow Graph for the state space matrix of SEPOSLC converter.

Input vector of your system coefficients:

i.e. [an an-1 an-2 ... a0] = [1 1.693e06 5.789e10 2.483e15 8.029e19 1.235e22]

Routh-Hurwitz Table:

rhTable =1.0e+22 *

0.0000	0.0000	0.0080
0.0000	0.0000	1.2350
0.0000	0.0080	0
0.0000	1.2350	0
0.0071	0	0
1.2350	0	0

~~~~~> it is a stable system! <~~~~~

Number of right hand side poles = 0

Do you want roots of system be shown? Y/N Y

Given polynomial coefficentsroots:

sysRoots=1.0e+06 *

-1.6590 + 0.0000i

-0.0333 + 0.0000i

-0.0003 + 0.0380i

-0.0003 - 0.0380i

-0.0002 + 0.0000i

From the above inferences, the proposed positive output super lift converter is stable by containing its negative poles of the system.

4. Description of Artificial Neural Network

Artificial Neural Networks (Figure 7) can be defined as computational models whose operation is based on parallel processing. The processing elements have some internal parameters called weights. By changing the weights, one can get practically any dynamic, linear or non-linear, behaviour of the transmission through the net [10].

Considering these properties, it has been suggested that neural networks can be useful as controllers for switch mode systems. The Artificial Neural Network Controller has been implemented for the proposed DC to DC converter using back propagation algorithm, delta learning rule, Hoffman adaptive neural scheme, wizhai training method and self-organizing map. The following steps are implemented by the ANN controller.

4.1 Training the neurons

- The acquired input is processed with the scalar variable ‘p’. Thus the input gets incremented for each feedback cycle.
- The processed data is then delayed for the specified duration by the delay unit. The delay is created by the presence of multiplexer in delay unit, which multiplexes the processed input again.
- In the weight unit, the delayed input is added up with weight value and dot product function of weight and bias is obtained. The dot product unit output is also multiplexed.
- The overall net sum of the output is applied to saturation unit, to check whether the linearized output meets the saturation condition or not.
- The obtained output is again processed with the scalar variable ‘p’. Thus the output gets corrected and get incremented for each feedback cycle. It is then given as output from ANN controller.

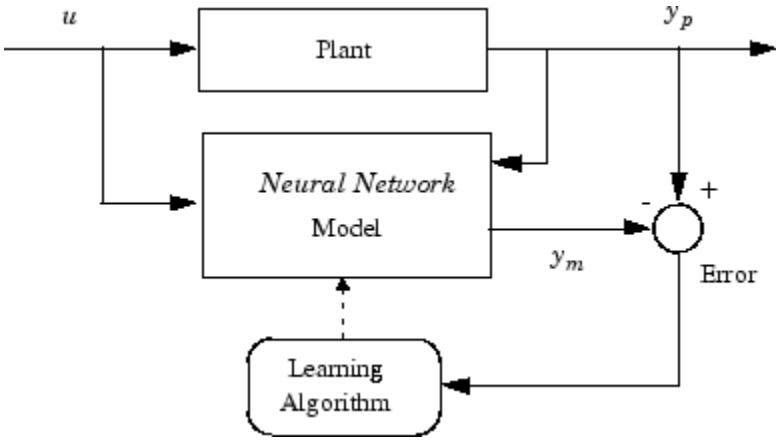

Figure 7. Basic building block of an artificial neural network controller.
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– The ANN controller output is then relationally compared with the repeating sequence signal.
– The compared output is given as gate signal to S2. The compared and inverted output is provided as a gate signal to S1.

The inputs given to the ANN controller are the actual output voltage obtained from the SEPOSLC and rate limited reference voltage. These two inputs are multiplexed, and the selected input is passed to ANN controller. Flow chart artificial neural network controller is shown in Figure 8.

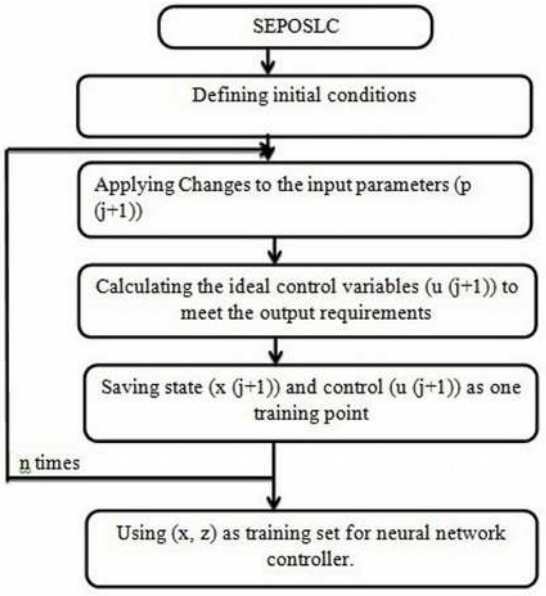

Figure 8. Flow chart artificial neural network controller.

Inside the ANN controller, the linear designing is implemented. The following steps are performed by the ANN controller. The acquired input is processed with the scalar variable ‘p'. Thus the input gets incremented for each feedback cycle.

The processed input is then delayed for the certain duration by the delay unit. The delay is created by the presence of multiplexer in delay unit, which multiplexes the processed input again.

In the weight unit, the delayed input is added up with weight value and dot product function of weight and bias is obtained. The dot product unit output is also multiplexed. The overall net sum of the output is applied to saturation unit, to check whether the linearized output meets the saturation condition or not.

The obtained output is again processed with the scalar variable ‘p'. Thus the output gets corrected and get incremented for each feedback cycle. It is then given as output from ANN controller. The ANN controller output is then relationally compared with the repeating sequence signal. The compared output is provided as a gate signal to S2. The compared and inverted output is given as gate signal to S1.

5. Simulation Results of SEPOSLC Converter

5.1 Line variation in SEPOSLC converter

The input voltage is varied from 8V to 6V and from 8V to 10V respectively, and their corresponding output voltage graph is obtained, in which the maximum overshoot is 0.15V and settling time is 0.005s as shown in Figure 9. The simulation results of line variation in SEPOSLC converter.

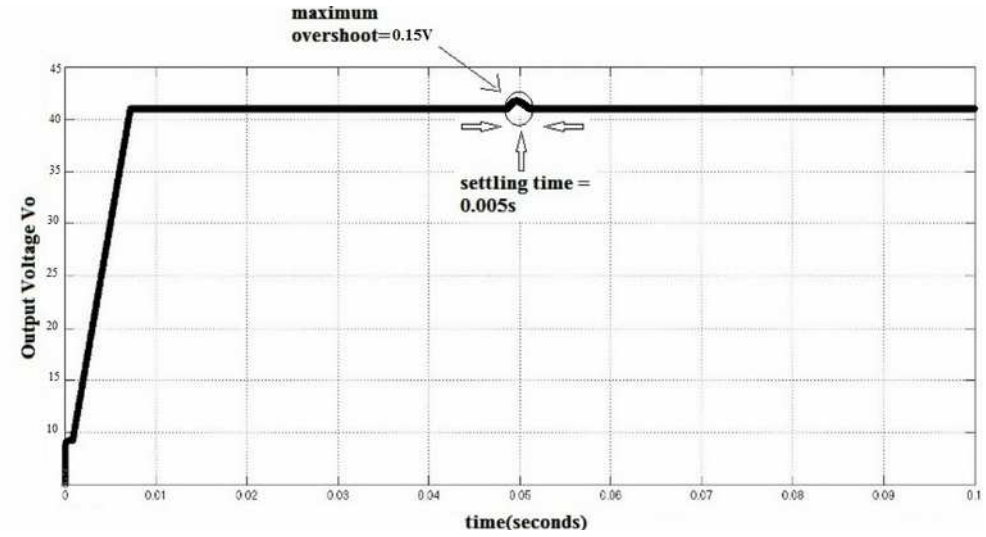

Figure 9. Output voltage during line variation of SEPOSLC converter.

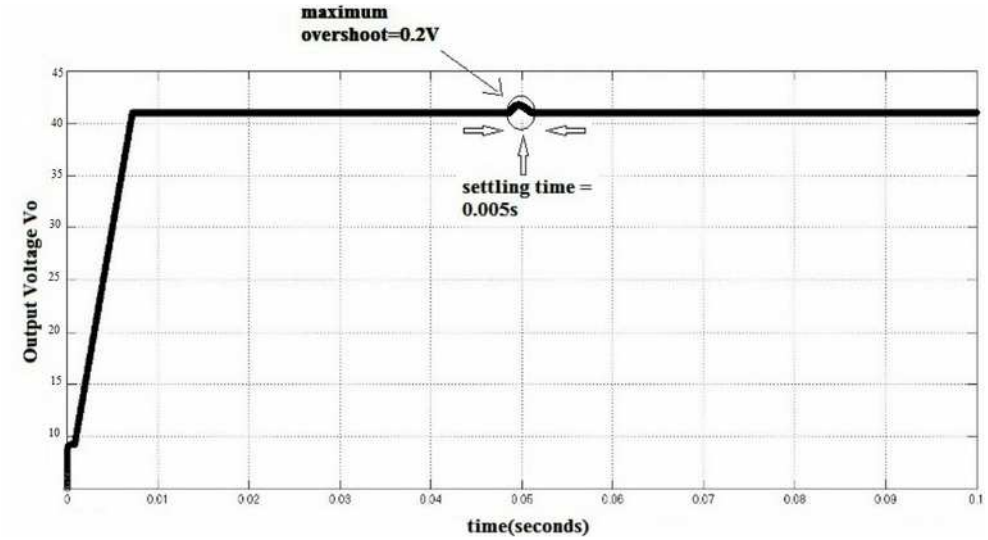

Figure 10. Output voltage during load variation of SEPOSLC converter.

5.2 Load variation in SEPOSLC converter

The load resistance is varied from 50Ω to 40Ω and from 50Ω to 60Ω respectively, and their corresponding output voltage graph is obtained, in which the maximum overshoot is 0.2V and settling time is 0.005s as shown in Figure 10. The simulation results of line variation in SEPOSLC converter.

6. Hardware Results of SEPOSLC Converter

6.1 Hardware kit for the proposed system

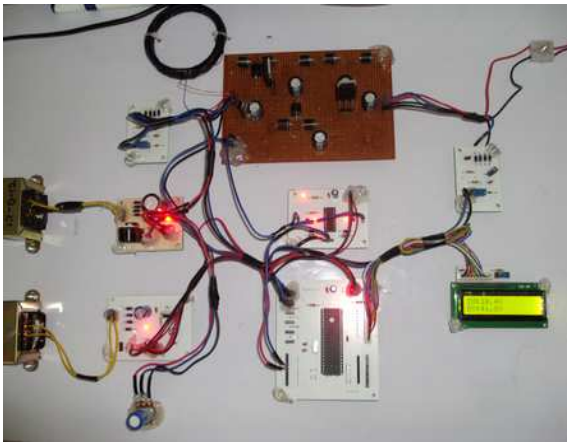

Figure 11. Output voltage during line variation of SEPOSLC converter.

The above Figure 11 shows the pictorial representation of SEPOSLC converter using ANNC controller. The hardware specification for the proposed system is implicated in the below Table 1.

Table 1. Hardware specification

S. No	Specification	Tool or Software
1	Embedded Controller	PIC16F887
2	Coding	Embedded C Language
3	C compiler	HITECH C
4	Simulator	MPLAB Simulator
5	Programmer	PIC KIT3 Programmer
6	Schematic Software (Circuit Designing)	Express Schematic
7	PCB Designing	Express PCB

6.2 Line variation in SEPOSLC converter

The input voltage is varied from 8V to 6V respectively, and their corresponding output voltage graph is obtained and shown in Figure 12, in which the maximum overshoot is 0.2V and settling time is 0.005s. The simulation results of line variation in SEPOSLC converter.

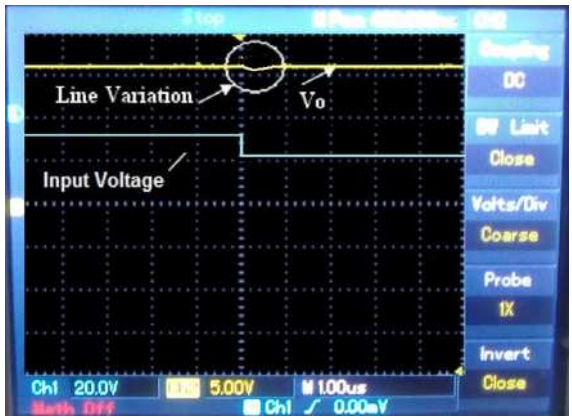

Figure 12. Output voltage during line variation of SEPOSLC converter.

The input voltage is varied from 8V to 10V respectively, and their corresponding output voltage graph is obtained and shown in Figure 13, in which the maximum overshoot is 0.2V and settling time is 0.005s. The simulation results of line variation in SEPOSLC converter.

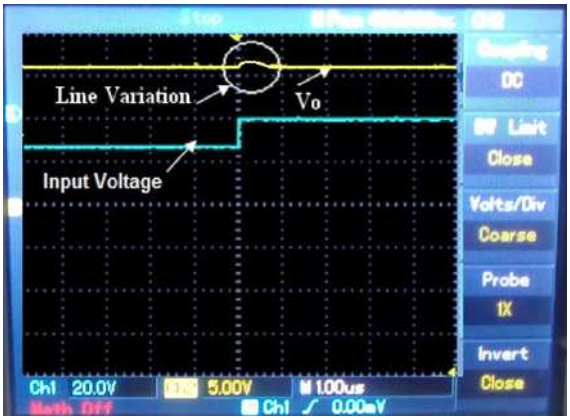

Figure 13. Output voltage during line variation of SEPOSLC converter.

6.3 Load variation in SEPOSLC converter

The load resistance is varied from 50Ω to 40Ω and respectively and their corresponding output voltage graph is obtained, in which the maximum overshoot is 0.15V and settling time is 0.005s as shown in Figure 14. The simulation results of line variation in SEPOSLC converter.

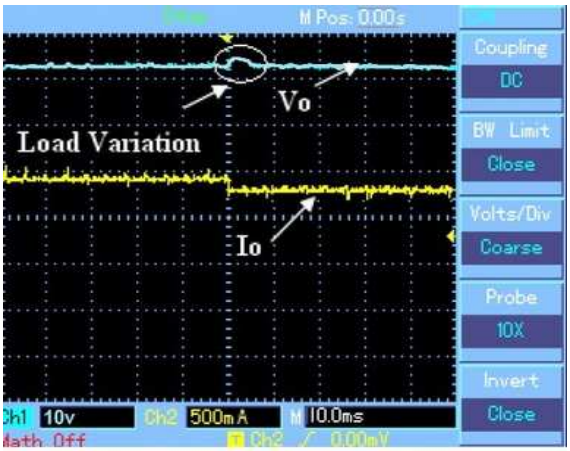

Figure 14. Output voltage during load variation of SEPOSLC converter.

The load resistance is varied from 50Ω to 60Ω respectively, and their corresponding output voltage graph is obtained and shown in Figure 15, in which the maximum overshoot is 0.15V and settling time is 0.005s. The simulation results of line variation in SEPOSLC converter.

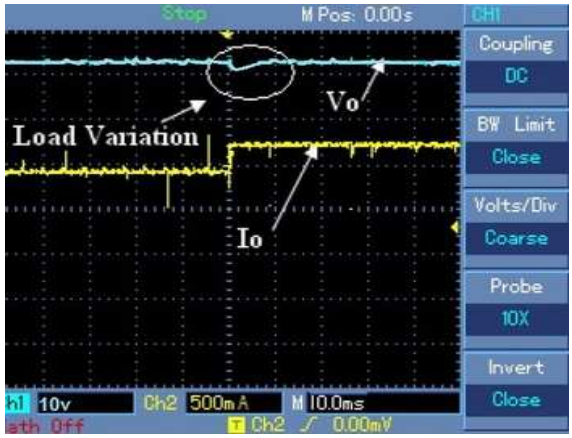

Figure 15. Output voltage during load variation of SEPOSLC converter.

6.4 Efficiency of the system in hardware

The efficiency of the above-described positive output super lift converter is calculated by using the formula

$$EFFICIENCY\ \eta = \frac{output\ power}{input\ power} * 100\,\%$$

$$EFFICIENCY\ \eta = \frac{input\ power\,(PE) - loses\,(EL)}{input\ power\,(PE)} * 100\,\%$$

$$EFFICIENCY\ \eta = 70.81\,\%$$

Therefore the obtained efficiency is lower, and the remaining 29.19% of efficiency is lagging due to the usage of more passive elements such as one inductor, six capacitor, two MOSFET switches and nine diodes. The overall power loss due to these passive elements is calculated using below formula.

$$Total\ Power\ Loss = w_{L1} + w_{c1} + w_{c2} + w_{c3} + w_{c4} + + w_{c5} + w_{sw1} + w_{sw2} + w_{D1\,to\,D7}$$

$$Total\ Power\ Loss = 29.19$$

6.5 Technical specification

Table 2 describes the essential parameters and its associated values for the SEPOSLC converter.

Table 2. Parameters list of SEPOSLC converter

Parameter list	Symbol	Value
Input Voltage	V_{in}	8V
Output Voltage	V_o	42V
Inductor	L	100µF
Capacitor	c_1 to c_s	30µF
Nominal Switching Frequency	f_s	100kHz
Load Resistance	R	50Ω
Range Of Duty Cycle	K	0.3 to 0.9
Desired Duty Cycle	K	0.5

6.6 Performance comparison of PI versus ANN controller

Table 3. Parameters list of SEPOSLC converter

TYPE	Line variation	Line variation	Load variation	Load variation
	8V to 6V	8V to 10V	50Ω to 40Ω	50Ω to 60Ω
PI	Maximum Overshoot =15V	Maximum Overshoot =15V	Maximum Overshoot =18V	Maximum Overshoot =18V
	Settling time =0.02s	Settling time =0.02s	Settling time =0.02s	Settling time =0.02s
ANN	Maximum Overshoot =0.2V	Maximum Overshoot =0.2V	Maximum Overshoot =0.1V	Maximum Overshoot =0.1V
	Settling time =0.005s	Settling time =0.005s	Settling time =0.005s	Settling time =0.005s

The bar chart representation of the above table is subjected below. Figure 16 represents the line, and load variation occurred in SEPOSLC converter using PI and ANN controller. Figure 17 represents the voltage transfer gain of various converters for subjective values of the duty cycle. From all the above inferences it proves the result that artificial neural network controller is the efficient and reliable for DC to DC converters than any other existing controllers.

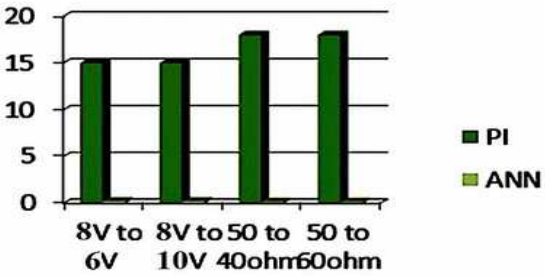

Figure 16. Represents line and load variation using PI and ANN controllers.

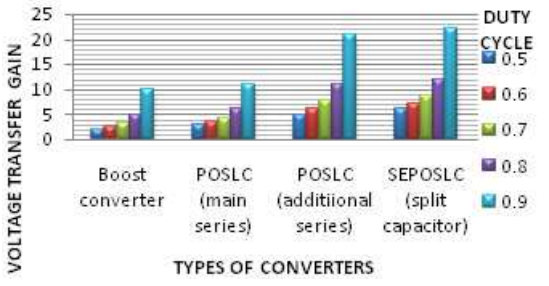

Figure 17. Represents voltage transfer gain for various converters.

7. Conclusion

Thus the Artificial neural network controller for positive output super lift converter has been implemented in hardware. Therefore the output voltage of the positive output super lift converter 41V is obtained for the low input voltage of 8V is achieved with very less negligible values of maximum overshoot and settling time. Finally, this ANNC for SEPOSLC system yields the better result with very less overshoot and settling time. Therefore the proposed system proves ANN controller is efficient and better than existing PI controllers. The SEPOSLC using ANN controller is proved to be stable for all essential conditions. This is achieved by the presence of artificial neural network controller in split capacitor type elementary additional series positive output super lift converter. The application of the ANNC controller may be a good alternative in circumstances requiring excellent regulation properties and exceptional dynamical response features.

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