Control of a Modular Multilevel Matrix Converter for High Power Applications

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Abstract: A control scheme for a multilevel AC-AC converter is presented. The converter resembles a matrix converter but it uses the cascade converter in place of converter valve. This is a string of H-bridge modules, each equipped with a DC storage capacitor, as the building block of the converter. This yields a highly modular implementation approach which may be suitable for high voltage, high power applications. One of the main issues with these modular multilevel converter topologies is the regulation of the capacitors voltages. This is a prerequisite to successfully operate the topology. This work explains the basics of the multilevel matrix converter and develops its associated control schemes to operate it as AC-AC converter. Control objectives include: regulation of multiple capacitor voltages; control of the multiple valve currents; and control of the output voltages. The proposed scheme is verified experimentally and through simulations. Results show good system performance in rejecting load impacts; maintaining capacitor voltages and valve currents within normal values; drawing low distortion, and close to unitary power factor, currents from the line; and creating high quality output voltages which result in low distortion load currents. The matrix multilevel converter thus shows great potential for high performance, high power motor drives.

Keywords: Modular multilevel converter, matrix converter, control of power converter

1. Introduction

Prerequisites

Because of the limitations of the current generation of semiconductor devices (voltage and switching frequency), large power converters typically use multi modular topologies such as the multi-pulse and multi-level converters [1]. In this context, because of the highly modular structure and the simplicity of the modules, the cascade converter is one of the most suitable topologies for high power applications [1]-[3], specially for Static Var Compensators, such as StatComs, and Active Power Filter (APF), where floating capacitors can implement the multiple isolated DC voltages needed.

At first, implementation of applications which requires the cascade converter to process active power, such as in a frequency changing converter [4], may not seem practical if implemented as a back-to-back connection of cascade converters. The requirement of isolation amongst the multiple H-bridge modules needs either multiple standard isolation transformers or a complex multi-winding isolation transformer [2] and [4].

Recently, a novel modular implementation approach to power converters, which resembles the direct AC-AC topology, as that shown in Figure 1 (no back-to-back based), has led to a new family of cascade-based converters [5]. This new generation of converters are known as the Modular Multilevel Converter (MMC) topology [5]-[6]. In this approach the cascade converter replaces the high-voltage valve (typically implemented by series IGBTs) required to implement a standard high-voltage converter topology. This is, for example, the series string of H-bridge converters arranged in a single-phase bridge, three-phase bridge or even in a full matrix converter topology.

The main advantages of MMC topologies come from using the multilevel conversion approach, with reduced switching frequency, hence reduced power losses, high quality input and output voltages and currents; and its highly modular implementation applying one of the simplest converter modules (the H-bridge converter). This may significantly reduce the cost of a high-power installation (manufacture of the modules and assemblage on the installation site).

One of the main challenges of this new conversion approach is in the development of suitable control strategies which enable these complex converter topologies to be used in a practical form (e.g. as a frequency changing converter). Tight control of the multiple capacitor voltages is fundamental to the successful operation of such converters.

This work addresses the control of a full matrix MMC topology. This is a converter which, as shown in Figure 1, has three input phases (*a*, *b* and *c*) and three output phases (*A*, *B* and *C*), where each switching element (valve) of the

matrix is a multilevel cascade converter. In particular, this manuscript develops a suitable control scheme to operate the converter of Figure 1 as a high performance AC-AC converter, capable of fast changing the amplitude, frequency and phase of the output voltages. This requires fast control of the valve currents, regulation of all of the capacitor voltages and fast control of the output voltages (to rapidly force the load currents, e.g. a motor). The remainder of this paper is organised as follows: Section 2 describes the basic operation of the cascade matrix converter; section 3 develops a dynamic model of the converter and develops the required control strategies, with emphasis on the regulation of capacitor voltages; and finally section 4 presents experimental and simulation results which demonstrate the performance of the converter to load impact.

2. Principle of Operation of the Converter

Figure 2 shows one section of the converter of Figure 1. The converter of Figure 2 uses two H-Bridge modules per valve. Clearly, the number of modules can be increased to increase the voltage rating, hence power, of the converter. The converter of Figure 2 implements a matrix converter which has three inputs and one output (3×1 matrix converter, e.g. a matrix converter involving the input phases *a*, *b*, *c* and the output phase *A*). This will be used to explain the operation of the full matrix converter and to develop its associated control system. The operation and control of the other two 3×1 matrix converters, which forms the 3×3 matrix converter, are similar to the one which is used as example case. The analysis which follows neglects the effect of switching of the power devices (voltages and currents do not contain high frequency ripple components due to the switching). The inductors in series with the valves are interface reactors, and like in a StatCom, are required to reduce the ripple current due to the switching. Compared to the valve voltage, the inductor voltage is small; and therefore can be neglected. Note that the DC side of each H-Bridge module in the valve is not connected to a power supply, or a load, so that it could be able to source/sink power to/from the AC side. Therefore, as in a StatCom, neglecting the converter losses, each valve is constraint to zero active power exchange with the rest of the system, otherwise capacitor voltages diverge (DC link voltage imbalance).

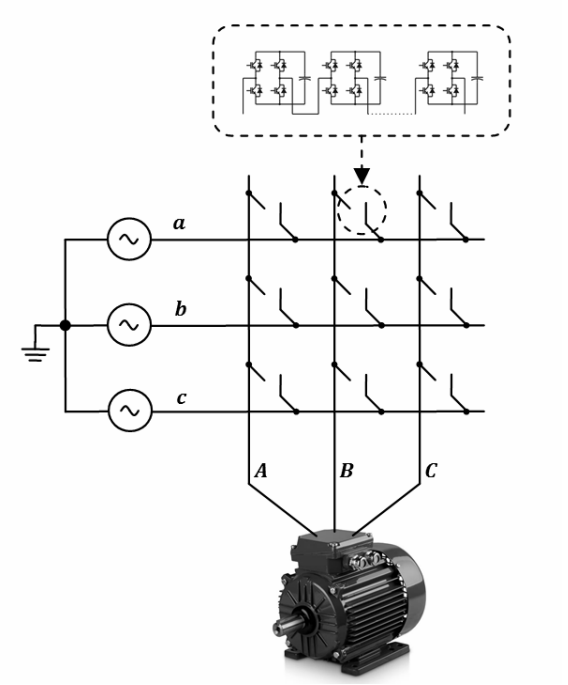

Figure 1 Cascade matrix converter

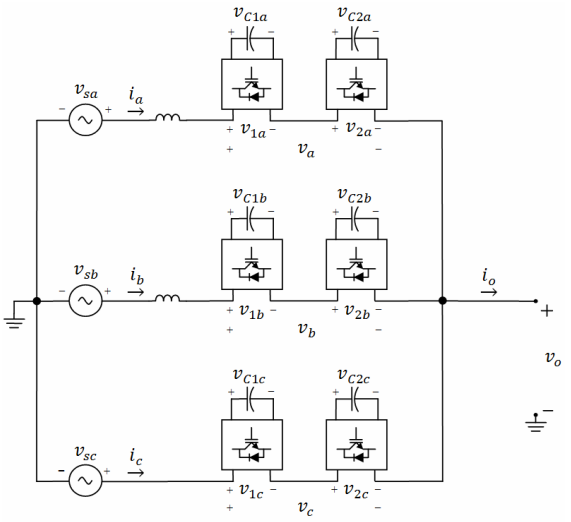

Figure 2. A 3×1 matrix converter (one phase of the full matrix converter).

As seen in Figure 2, each valve is placed between a particular input and particular output of the converter. Therefore, to output a given converter voltage, the multilevel converters (valves) of Figure 2, are required to produce the voltage difference between the corresponding input and output terminal (e.g. $v_a = v_{1a} + v_{2a} = v_{sa} - v_o$). If capacitor voltages are sufficiently high, any voltage demand, within converter ratings, can be set using a suitable modulation strategy (e.g. multilevel PWM based modulation strategies). To maintain capacitor voltages stable, assuming

well balanced capacitor voltages, the active power exchanged by each valve with the system is required to be zero. In general, the valve voltage and valve current contain two frequency components, one at the input frequency (ω_s) and the other at the output frequency (ω_o), assumed to be different to the input frequency (frequency changing). It can be shown that the mean power of a valve is given by (1).

$$P_{val} = \frac{1}{2}\left(V_{s\_val}\, I_{s\_val} - V_{o\_val}\, I_{o\_val}\right) \quad (1)$$

Where V_{s_val} is the amplitude of the voltage component at the input frequency and I_{s_val} is the amplitude of the current component which is in phase with the input voltage. Similarly, V_{o_val} is the amplitude of the valve voltage at the output frequency, and I_{o_val} is the amplitude of current component in phase with the output voltage. The active power due to the voltage and current components which are at the input frequency should balance the active power due to the voltage and current components which are at the output frequency, i.e. $P_{val} = 0 \rightarrow V_{s\_val}\, I_{s\_val} = V_{o\_val}\, I_{o\_val}$. In this scheme balance of the active power is achieved by a control system which adjusts the amplitude of the input current in according to the deviation of the capacitor voltages with respect to its reference value (DC link voltage regulation sub-system). It is anticipated that the balance between the input and output power is achieved by adjusting the amplitude of the positive sequence component which is in phase with the input voltages; whereas the unbalance amongst the stored energy in the valves (stored in the capacitors of the valve) are corrected exchanging energy amongst the various valves without affecting the balance between the input and output power. This is accomplished by adjusting the negative sequence components of the input current (the in phase and quadrature negative sequence components).

3. Control Strategy

This section develops the control strategies to: 1) regulate the capacitor voltages of each valve; 2) force the valve currents; and 3) set the output voltage. To this end, a simplified dynamic model of the converter is developed next. For simplicity dynamics of capacitor voltages is expressed in terms of the stored energy in the capacitor instead of the capacitor voltage itself. Further, it is assumed that each valve current closely follows its respective reference, as dictated by the corresponding DC capacitor voltage controller. Therefore, dynamics of the valve current can be neglected. In this particular application the valve current is forced by a dead-beat controller [7]. The dynamics of the stored energy in the capacitor of an H-bridge module is given in (2). Neglecting the losses, (2) represents the balance between the instantaneous AC-side and DC-side power of the module.

$$\frac{dW}{dt} = p = v\, i \quad (2)$$

Where v is the AC-side voltage of the H-bridge module, i is the current which flows through this module and W is the stored energy in the DC storage capacitor.

Considering the voltages and currents of Figure 2, the dynamics of capacitors is given in (3).

$$\begin{aligned} \frac{dW_{1a}}{dt} &= v_{1a}\, i_a & \frac{dW_{2a}}{dt} &= v_{2a}\, i_a \\ \frac{dW_{1b}}{dt} &= v_{1b}\, i_b & \frac{dW_{2b}}{dt} &= v_{2b}\, i_b \\ \frac{dW_{1c}}{dt} &= v_{1c}\, i_c & \frac{dW_{2c}}{dt} &= v_{2c}\, i_c \end{aligned} \quad (3)$$

An increase in the capacitor voltage requires the H-bridge module to draw energy, hence power, from the rest of the system and deliver it to the capacitor; and vice-versa to reduce the capacitor voltage. This can be achieved by manipulating either the H-bridge module voltage or current, or both.

Like in a cascade StatCom, control of capacitor voltages in each particular valve can be described as two control objectives which can be decoupled [8].

1. Regulation of the sum of the capacitor voltages, hence total stored energy, of the valve.
2. Equalisation of the capacitor voltages of the valve (typically known as balancing of the capacitor voltages).

Using (3), the total stored energy on each valve (e.g. $W_a = W_{1a} + W_{2a}$, for phase *a*), and the unbalance amongst the stored energy in the

modules of the valve ($\Delta W_a = W_{1a} - W_{2a}$) are given in (4).

$$\begin{aligned}
\frac{dW_a}{dt} &= (v_{sa} - v_o) i_a \\
\frac{dW_b}{dt} &= (v_{sb} - v_o) i_b \\
\frac{dW_c}{dt} &= (v_{sc} - v_o) i_c \\
\frac{d\Delta W_a}{dt} &= (v_{1a} - v_{2a}) i_a \\
\frac{d\Delta W_b}{dt} &= (v_{1b} - v_{2b}) i_b \\
\frac{d\Delta W_c}{dt} &= (v_{1c} - v_{2c}) i_c
\end{aligned} \tag{4}$$

One of the main issues of the proposed converter is the control of the total capacitor voltage of each valve. Like in a cascade StatCom, equalisation of the multiple capacitor voltages in each valve can be achieved by injecting, on each H-bridge module, a small voltage component which is in-phase/anti-phase with the valve current [8]. By doing so, equalisation of capacitor voltages is decoupled from the regulation of the total capacitor voltage. This reduces the order of the dynamics of the modular multilevel converter from a very high order system to a low order system, but still far more complex than that of a standard converter which uses a single DC storage capacitor. Note that a high voltage converter will typically require hundreds of H-bridge modules.

In developing the control scheme of the total capacitor voltage of the valves, only the first three equations of (4) are required. This is a third order system and its associated control sub-system can be approached as a problem of regulating the total stored energy in the converter of Figure 2, this is the three valves; and balancing the stored energy amongst the three valves. It can be shown that using the state variables in (5), the dynamic of the total stored energy in the valves can be expressed as given in (6).

$$\begin{aligned}
W_T &= W_a + W_b + W_c \\
W_\alpha &= W_a - \frac{1}{2} W_b - \frac{1}{2} W_c \\
W_\beta &= W_b - W_c
\end{aligned} \tag{5}$$

$$\begin{aligned}
\frac{dW_T}{dt} &= \frac{3}{2} V_s I_T \\
\frac{dW_\alpha}{dt} &= \frac{3}{4} V_s I_\alpha \\
\frac{dW_\beta}{dt} &= \frac{\sqrt{3}}{2} V_s I_\beta
\end{aligned} \tag{6}$$

Where V_s is the amplitude of the input voltage, I_T is the amplitude of the positive sequence component in phase with the input voltage of phase *a*, I_α is the amplitude of the negative sequence component in phase with phase *a*, and I_β is the amplitude of the negative sequence component in quadrature to phase *a*.

Assuming that capacitor voltages are close to its reference voltage (nominal DC voltage), $v_{C1a} = v_{C2a} = v_{C1b} = v_{C2b} = v_{C1c} = v_{C2c} \approx V_C$, the dynamic of capacitor voltages is given by (7).

$$\begin{aligned}
\frac{dV_T}{dt} &= \frac{3V_s}{2CV_C} I_T \\
\frac{dV_\alpha}{dt} &= \frac{3V_s}{4CV_C} I_\alpha \\
\frac{dV_\beta}{dt} &= \frac{\sqrt{3}V_s}{2CV_C} I_\beta
\end{aligned} \tag{7}$$

Where *C* is the capacitance of the DC capacitor of the H-bridge module, assumed equal for all modules, and V_C is the nominal DC voltage of the module.

From (7), it follows that the total capacitor voltage can be controlled by injecting an in-phase-positive sequence current; whereas the unbalance between the total capacitor voltage of valve *a* and valve *b* and *c* (*b*-*c* as a pair) can be controlled by injecting an in-phase-negative sequence component; and unbalance between the total capacitor voltage of valve *b* and valve *c* can be controlled by injecting an in-quadrature-negative sequence current. This implements a decoupled control scheme of the total capacitor voltages but in the form of an overall capacitor voltage and two voltage deviations. Note that (7) represents three independent (decoupled) first order systems, therefore, their corresponding controllers can design in a separate way.

Figure 3 shows a simplified block diagram of the control system which regulates the total

capacitor voltage of the three valves. The capacitor voltages of each valve are first summed, to calculate the total capacitor voltage of each valve, and then transformed according to (5) and fed back into the PI controllers which, according to the voltage error, set the amplitude of the various components of the input current (positive in-phase and negative in-phase and in-quadrature). The outputs of the PI controller are multiplied by sinusoidal signals of unitary amplitude, and of the appropriate phase and sequence, to shape the control actions into sinusoidal reference currents, as given in (8).

$$\begin{aligned} i_a^* &= I_T\, u_a - I_\alpha\, u_a + I_\beta \left(u_b - u_c\right) + i_o / 3 \\ i_b^* &= I_T\, u_b - I_\alpha\, u_c - I_\beta \left(u_b - u_c\right) / 2 + i_o / 3 \end{aligned} \tag{8}$$

Where u_a, u_b and u_c are sinusoidal signals of unitary amplitude in phase with the input voltage of phase *a*, *b* and *c*, respectively.

with

$$I_{T\_total} = I_{TA} + I_{TB} + I_{TC}$$

$$I_{\alpha\_total} = I_{\alpha A} + I_{\alpha B} + I_{\alpha C}$$

$$I_{\beta\_total} = I_{\beta A} + I_{\beta B} + I_{\beta C}$$

Where I_{TA}, I_{TB} and I_{TC} are, respectively, the amplitude of the positive sequence current set by the capacitor voltage controller of phase *A*, *B* and *C*. Similarly, $I_{\alpha A}$, $I_{\alpha B}$ and $I_{\alpha C}$ are the amplitude of the in-phase negative sequence current set by the capacitor voltage controllers; and $I_{\beta A}$, $I_{\beta B}$ and $I_{\beta C}$ are the amplitude of the in-quadrature negative sequence current set by the capacitor voltage controllers.

In (9), i_{oA}, i_{oB} and i_{oC} are, respectively, the current of the output phase *A*, *B* and *C*. Note that these currents are fed forward as reference

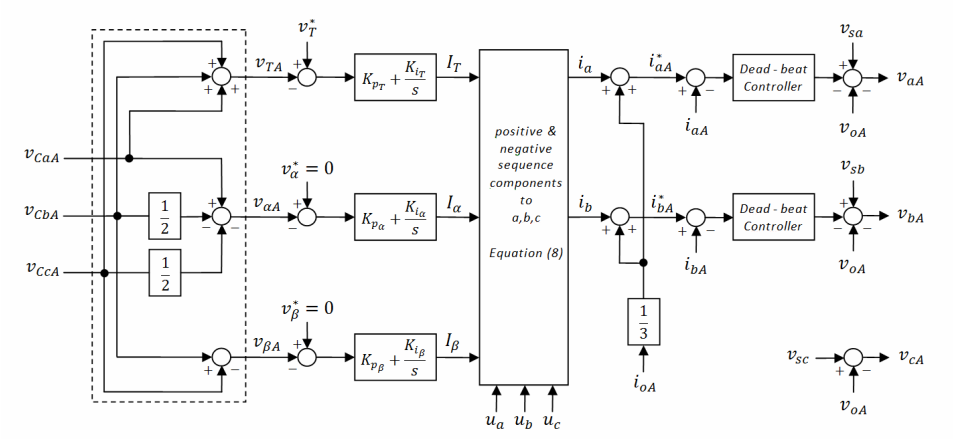

Figure 3. A simplified control system block diagram for the converter of Figure 2.

As mentioned in section 2, the control scheme described above applies to a section of the of the full matrix converter. Three controllers similar to that in Figure 3 are required to control the full matrix converter. The reference currents in (8) represent the contribution of one of the output phases to each of the input phase currents. Therefore, assuming perfect tracking of the reference currents, the total input phase currents (considering the three controllers) are given in (9).

$$\begin{aligned} i_a &= I_{T\_total}\, u_a I_{\alpha\_total}\, u_a + \\ &\quad I_{\beta\_total} \left(u_b - u_c\right) + \left(i_{oA} + i_{oB} + i_{oC}\right) / 3 \\ i_b &= I_{T\_total}\, u_b - I_{\alpha\_total}\, u_c - \\ &\quad I_{\beta\_total} \left(u_b - u_c\right) / 2 + \left(i_{oA} + i_{oB} + i_{oC}\right) / 3 \end{aligned} \tag{9}$$

to the input phase currents. Therefore, the term $\left(i_{oA} + i_{oB} + i_{oC}\right) / 3$ in (9) represents the contribution of the output currents to each of the phase input current. This contribution actually corresponds only to the zero-sequence component of the output currents. For balanced loads or 3-wire loads (no neutral) the zero sequence current is zero. Therefore, the load currents cancel out from the input currents, thus remaining only the components which are at the input frequency (line frequency). The phase input currents are expected to be nearly sinusoidal currents. Further, for balanced loads, the required negative sequence current components (in-phase and in-quadrature) will be small and therefore the converter is able to operate at near unity power factor.

4. Results

To validate the proposals, a low power prototype of the converter of Figure 2, but having only one H-bridge module per valve, was built and tested for load impacts while it operates as a frequency changing converter from 50 Hz to $16^{2/3}$ Hz. This low frequency output ($16^{2/3}$ Hz) is typical in distribution of electricity to railways systems. This section presents some experimental results of system response to load impact. Simulation results which confirm operation of the a full matrix converter having two H-bridge modules per valve, hence 18 H-bridge in total, are also presented.

Figure 4 shows a photograph of the experimental system. The H-bridge modules use 100 V, 50 A MOSFETs as switching device, switching at 1 kHz. The DC capacitor voltage is set to 50 V. The prototype converter is controlled by a DSP DSK 6713 board equipped with a daughter board which implements an analogue interface and PWM units. The parameters of the PI controllers of Figure 3 are chosen so that the voltage regulation loop has a response time of 200 ms.

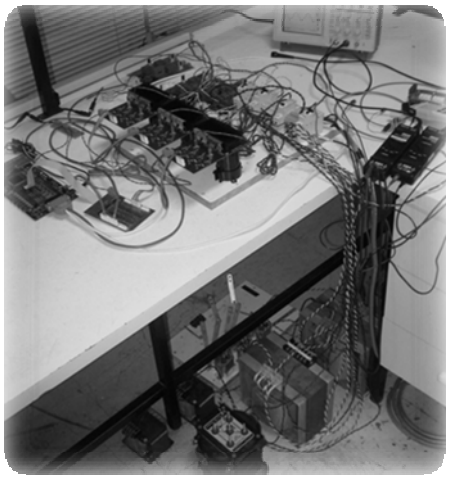

Figure 4. A photograph of the experimental system.

4.1 Results load impact test

This section presents the system response to load impacts when the experimental system operates as a $16^{2/3}$ voltage source, to feed an R-L load, while supplied from a 50 Hz system. In this test a switched R-L load is used to apply load steps from zero to full load and back again. Figure 5 shows system response when the load is shed on and it includes: phase input voltages and currents; reference output voltage and load current; and the capacitor voltage of the three H-bridge modules. The results of Figure 5 correspond to voltages and currents as sampled, every 500 us, by the control system. Therefore, Figure 5 does not generally show the effect of switching of the power converters. Experimental steady-state converter voltages and currents waveforms, as captured by a digital storage scope, are shown in Figure 6.

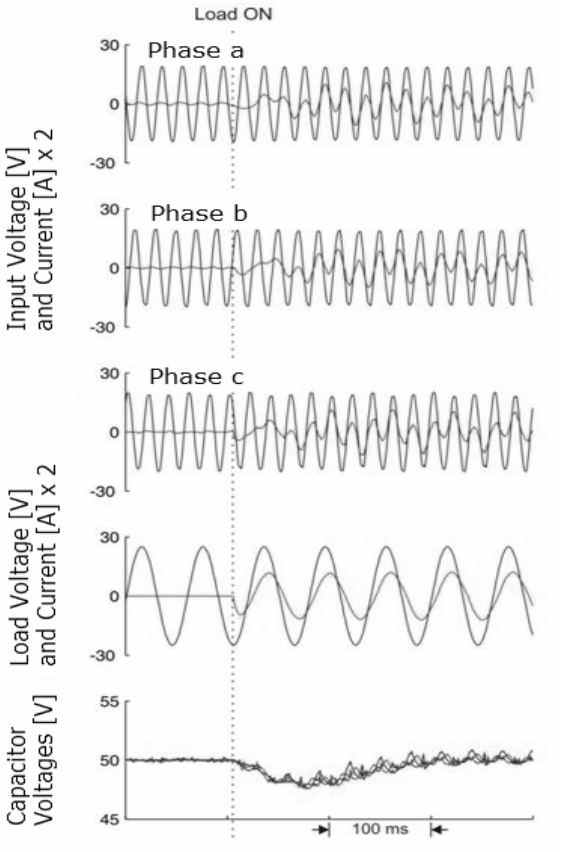

Figure 5. System response to a load impact when frequency changing operates a power supply at 162/3 Hz output.

As seen from Figure 5, following the load step, the capacitor voltage of all three H-bridge modules start dropping but recover, as expected from design specifications of the capacitor voltage controllers, within 200 ms.

Figure 6 shows the voltage and current of phase *a* along with the PWM voltage of the H-bridge module of this phase. As expected, the phase current is a complex current waveform which contains components at the input frequency (50 Hz) and the output frequency ($16^{2/3}$ Hz). The voltage across the H-bridge is a three-level PWM voltage waveform. This voltage forces the phase a current. Therefore, in addition to the high frequency components (due to the switching), the H-bridge voltage contains the 50 Hz and $16^{2/3}$ Hz frequency components.

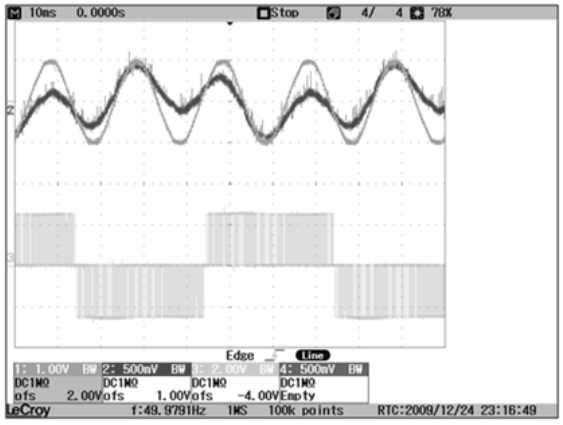

Figure 6. Voltage and current phase a (top). Scale: 20 V/div and 5 A/div. H-bridge converter voltage phase a (bottom). Scale: 40 V/div.

Figure 7 (top) shows that the capacitor voltage of the H-bridge of phase *a*, *b* and *c* are well balanced and, as expected, kept at 50 V, thus confirming a good performance of the proposed control system. For the purpose of synchronisation, Figure 7 also shows the load current. This is repeated in Figure 8 but now along with the output voltage. As seen from Figure 8, the quality of the load current is very high (nearly sinusoidal). The waveform of the output voltage is not common in standard converters. However, neglecting the high frequency components, this voltage waveform should contain only the $16^{2/3}$ Hz component. This claim is supported by the high quality of the load current.

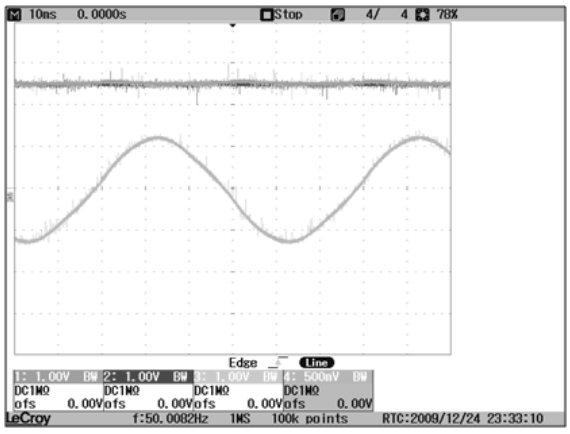

Figure 7. Capacitor voltages (top). Scale: 20 V/div. Load current (bottom). Scale: 5A/div.

In general, the results of Figure 5 to Figure 8 demonstrate good operation of the converter under the proposed control system, with an excellent performance in rejecting load disturbances; capacitor voltages well regulated; valve currents within normal operation values; and small ripple current, as expected from a converter which uses PWM modulation technique.

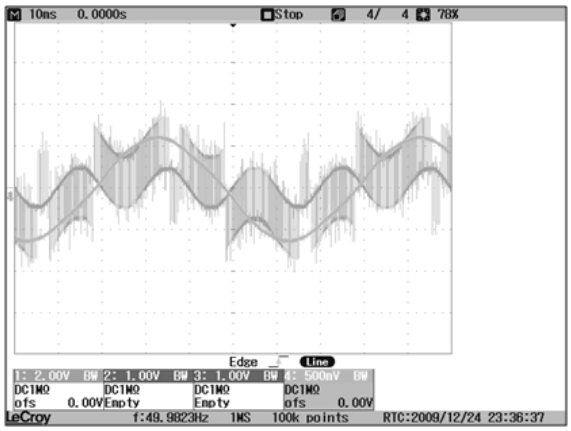

Figure 8. Load voltage and current. Scale: 40 V/div and 5 A/div.

4.2 Simulation of the full matrix MMC

To further verify other aspects of the operation of the converter such as balancing of the capacitor voltages and its ability to operate at near unity power factor, a simulation study in PSIM (simulation software for conversion and control) was carried out. The study uses a detailed converter model of the full matrix topology (3×3 matrix converter), in this case using two H-bridge modules per valve. Therefore, the overall converter uses 18 H-bridge modules. Figure 9 shows system response to a load step similar to that of Figure 5. Note that there is only a small

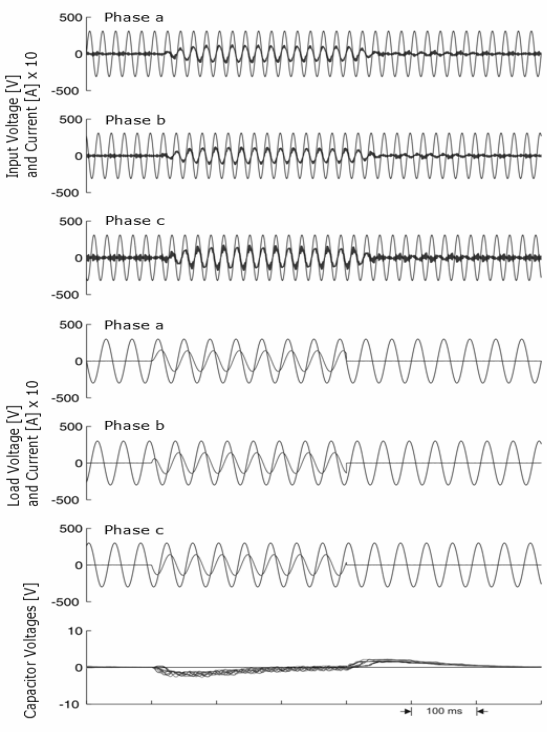

Figure 9. Simulation load impact full matrix converter (18 H-bridge modules). DC capacitor voltages correspond to the voltage deviation with respect to the reference DC voltage.

difference amongst the 18 capacitor voltages of the converter. Note also that unlike the experimental results, which represent only one output phase of the full matrix converter, the input currents are nearly sinusoidal. This is because the current of phase *A*, *B* and *C* (output phases), which flow through the valves, neutralise each other at the input phases (phase *a*, *b* and *c*).

5. Conclusions

The operation of a frequency changing converter which uses the cascade converter in its simplest form (equipped only with a capacitor on its DC-side) as converter valve was successfully demonstrated. To this end, the various control strategies needed for proper operation of this complex converter topology were developed.

The proposals have been demonstrated experimentally and through simulations. The results show that the proposed control scheme is very robust and has an excellent performance in rejecting load disturbances; while regulating all the capacitor voltages and maintaining valve current within normal operation values. The MMC matrix converter can provide high quality output voltage waveforms and can draw low distortion currents from the line, at close to unity power factor, thus facilitating interfacing to the load and the line.

In MMC topologies, the cascade converter, hence H-bridge module, is used as a building block. This enables modular implementation approach in which voltage rating, hence power rating, can be readily extended to higher values by adding as many H-bridge modules as required to meet voltage and power rating of the application.

Therefore, the modular matrix converter is an interesting alternative to implement high power frequency changing converters and variable frequency converters which may be suitable for motor drives.

Acknowledgements

The authors would like to acknowledge the support of the Chilean Government through the Research Grant Fondecyt-1071136.

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